

Exhibit 8

Exhibit A-1 to Greenthread’s Complaint (U.S. Patent No. 10,510,842)




| U.S. Patent No. 10,510,842 | Exemplary Accused Product Cirrus Logic CLI1793B1 Power Management Integrated Circuit |
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| <p>[Claim 1, Preamble] A semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products constitute and are incorporated into semiconductor devices. This chart includes exemplary information regarding a representative example of the Cirrus Logic CLI1793B1 power management integrated circuit (“PMIC”) (“CLI1793B1”) used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The CLI1793B1 was analyzed in the below referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed in Exhibits A-1 through A-6. Selected pages are reproduced herein to aid in understanding. https://www.techinsights.com/products/pef-2110-802</p> <div data-bbox="300 435 1740 1250"><h3>Apple iPhone 13 Pro – Photograph & Main Printed Circuit Board</h3><ul style="list-style-type: none">The PMIC device component (338S00817) was extracted from the main PCB of the Apple iPhone 13 Pro smartphone, as outlined in the image below [3].<div><p>A2484_1E_Thumbnail.png</p></div><div><p>img54447.png</p></div><div></div></div> <p>10 All content © 2022 TechInsights Inc. All rights reserved.</p> <p>The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the ’842 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the ’842 patent (and the other asserted patents). The</p> |

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| | <p>claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> |
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| | <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Cirrus Logic Accused Products, of which Cirrus Logic CLI1793B1 is one example, are semiconductor devices.</p> |
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¹ https://www.cirrus.com/products/#psearch_T200

² https://www.cirrus.com/products/#psearch_T100

³ https://www.cirrus.com/products/#psearch_T400

⁴ https://www.cirrus.com/products/#psearch_T300

⁵ https://www.cirrus.com/products/#psearch_T800

⁶ https://www.cirrus.com/products/#psearch_T3000

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Power Block SPM/sMIM Analysis – Cross-Section

- The higher magnification SPM/sMIM images show a large N-doped block under the drain that is located farther from the gate, supportive of the DeMOSFET structure.
- Under the source, there are blocks of highly P-doped wells, which appear to be on top of a lightly P-doped layer. This P-doped layer is of course located on top of the buried N-well.

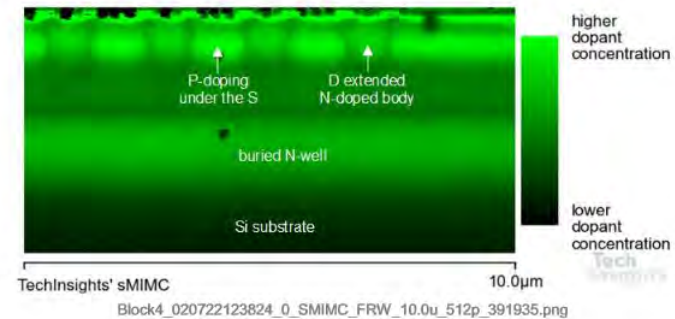
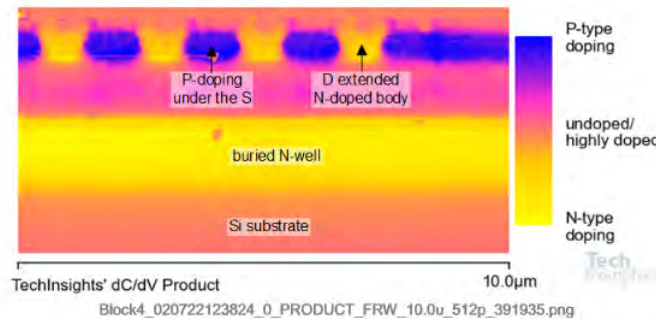


Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Device Summary

- This report presents an analysis of the Cirrus Logic CLI1793B1 die within the Apple 338S00817 that is a silicon-based power management integrated circuit (PMIC) die. The CLI1793B1 die is housed in a wafer level package (WLP), 338S00817, designed by Cirrus Logic. The 338S00817 component was extracted from the main PCB of the Apple iPhone 13 Pro smartphone.
- The CLI1793B1 die is approximately 290 μm thick. It contains a large logic region towards its right area, whereas there are several regions occupied with (nearly identical, i.e. similar pitches and visual configurations) power blocks.
- The logic and power blocks, both feature a two-layer passivation (with a significant variable thickness, 0.17-0.91 μm), six layers of metal interconnect (one aluminum (Al) top metal layer and six copper (Cu) metal layers), tungsten (W) contacts, STI, and silicided polysilicon gate transistors.
- The power transistors are a form of LDMOS, likely a drain extended MOSFET (DeMOSFET) structure, where there are three small N-wells under the source within a large, lightly P-doped body, narrow P-doping under the gate, and an extended block of N-doped body under the drain. The extended body under the drain appears to be made of lighter doping interior and highly N-doped walls.
- The silicon (Si) die features one buried N-well (approximately 1.8 μm) between the P-doped body on top and (lightly doped) Si substrate. The MOSFET die uses a two-layer passivation made of a ~ 0.5 μm SiN outer and ~ 0.5 μm SiO inner layer, silicon oxide (SiO) pre-metal dielectric (PMD) layers, and a SiO gate dielectric. The polysilicon gates are ~ 70 nm thick, topped with NiSi (~ 29 -32 nm), and a SiN contact etch stop layer (CESL; ~ 31 -33 nm).

| | |
|---------------------------|---|
| Manufacturer | Apple |
| Part number | 338S00817 |
| Type | PMIC |
| Date code | 2125 (week 25 of 2021) |
| Package type | Wafer level package (WLP) |
| Package markings | 338S00817 RDWBB1AO2125 TW NQJQL |
| Package dimensions | 3.7 mm \times 5.1 mm \times 0.5 mm thick |
| Die markings | CIRRUS LOGIC 2021 <logo> CLI1793B1 B69 CS37L10R06 B0 |

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Power Block SPM/sMIM Analysis – Cross-Section

- The SPM/sMIM data shows a buried N-well layer (likely not epitaxially grown layers due to its non-uniformity on the Si substrate) formed on the Si substrate top. sMIM image on the right suggests that this layer is comprised of two sublayers, with the one closer to the Si substrate with a higher level of doping.
- The DeMOSFET layer is also made of sequences of S and D, with S characterized from its triple contacts (NiSi) on the sMIM image, whereas that of the drain is singular.
- Note that SCM imaging (such as the left image) is sensitive to the dopant type, with N-type material giving a negative (yellow) response, and P-type material giving a positive (purple) response.
- sMIM imaging (such as the right image) is sensitive to the dopant concentration level, with greater signal (brighter) corresponding to a higher dopant level, regardless of conductivity type.

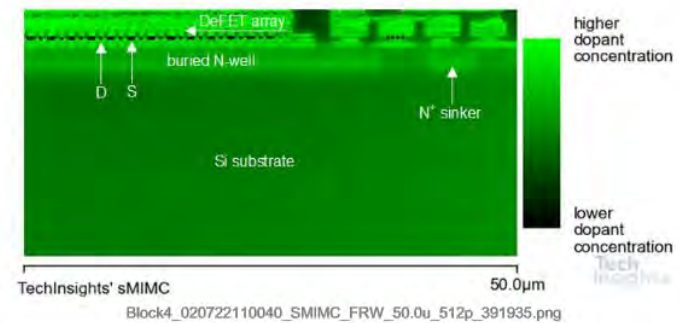
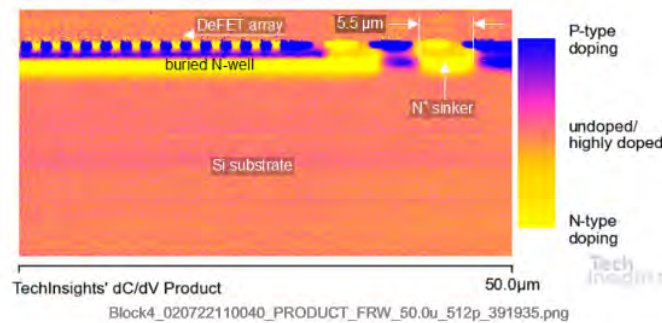


Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Power Block SPM/sMIM Analysis – Cross-Section

- The higher magnification SPM/sMIM images show a large N-doped block under the drain that is located farther from the gate, supportive of the DeMOSFET structure.
- Under the source, there are blocks of highly P-doped wells, which appear to be on top of a lightly P-doped layer. This P-doped layer is of course located on top of the buried N-well.

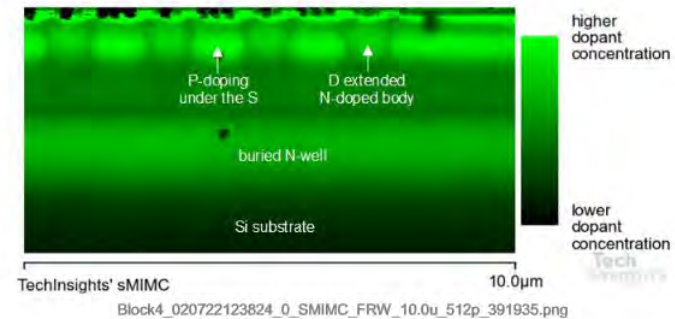
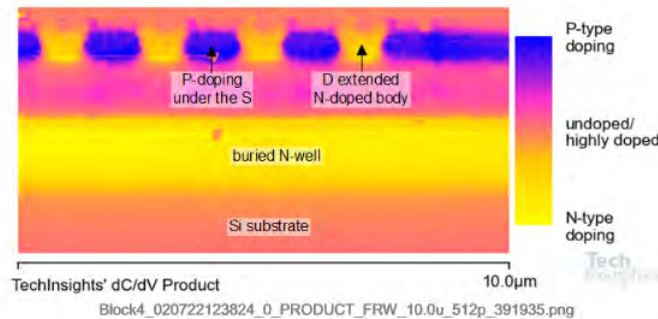


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Power Block SPM/sMIM Analysis – Cross-Section

- The buried N-well appears to consist of two sublayers:
 - The top layer with lighter N-doping is 1.0 μm thick.
 - The bottom layer has a higher N-doping with 0.8 μm thickness.
- For each source, one can see two gates with P-doping underneath surrounding the source. The source appears to have a narrow N-doped layer, while drain is embarked on top of a large N-doped well.

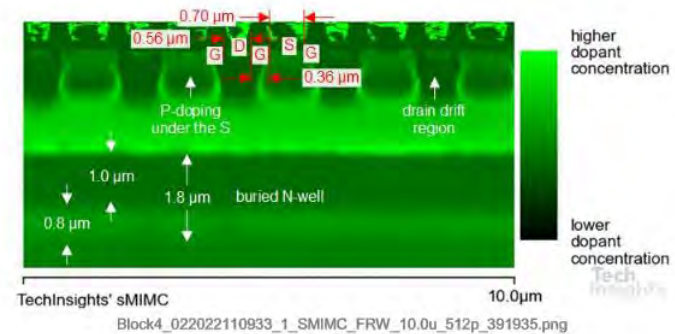
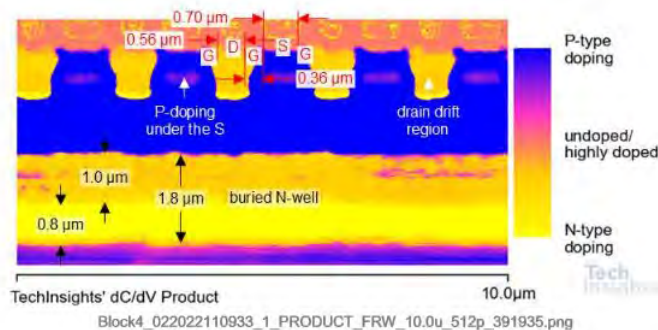
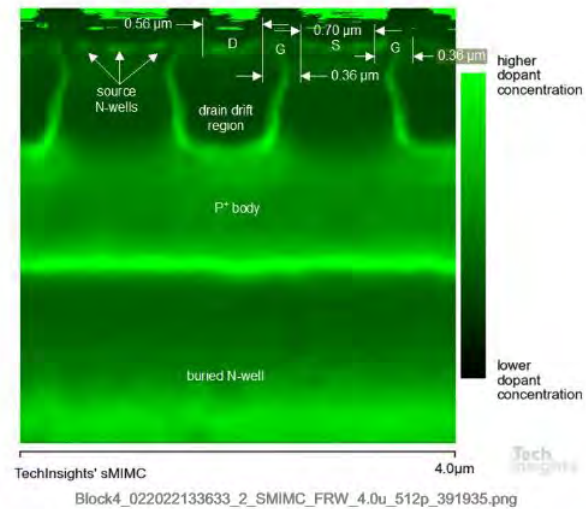
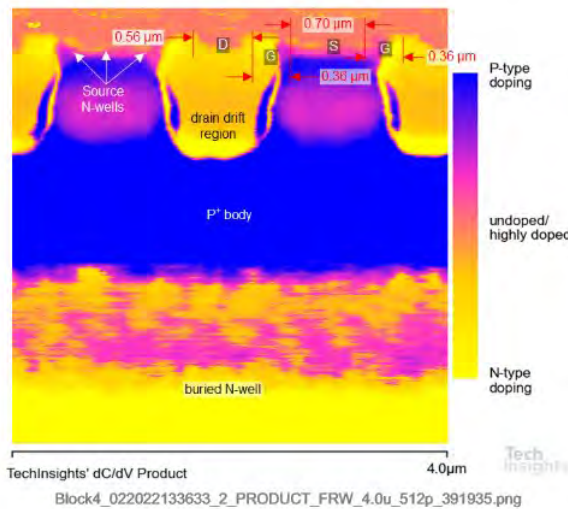


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Power Block SPM/sMIM Analysis – Cross-Section

- Here one can (more) safely claim to see three source N-wells within the large P-well under the source. These are more obvious in the sMIM. The gates are on small P-doped wells, located closer to the source. These observations appear consistent with a DeMOSFET structure.



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[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;

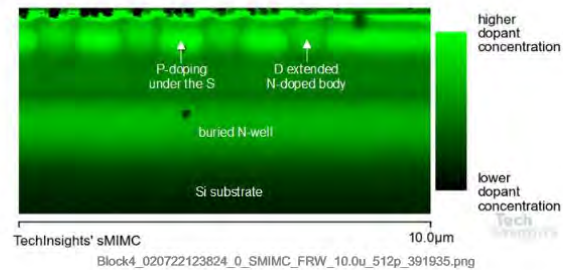
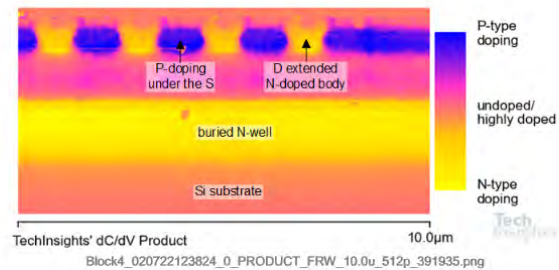
The Cirrus Logic Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Cirrus Logic Accused Product (the Cirrus Logic CLI1793B1 discussed above) incorporated into an exemplary Cirrus Logic PMIC reveals the presence of such a substrate.

For example, the Cirrus Logic CLI1793B1 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning probe/capacitance/microwave impedance microscopy (SPM/SCM/sMIM) analysis.

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Power Block SPM/sMIM Analysis – Cross-Section

- The higher magnification SPM/sMIM images show a large N-doped block under the drain that is located farther from the gate, supportive of the DeMOSFET structure.
- Under the source, there are blocks of highly P-doped wells, which appear to be on top of a lightly P-doped layer. This P-doped layer is of course located on top of the buried N-well.



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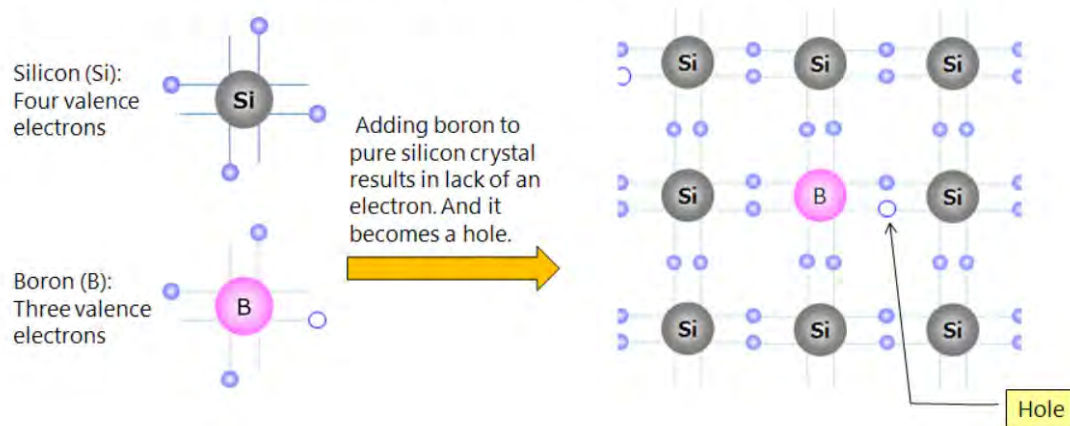
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Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

What is a p-type Semiconductor?

A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "-" electrode in sequence.



* This hole is the carrier of a p-type semiconductor.

See <https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.>

[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which

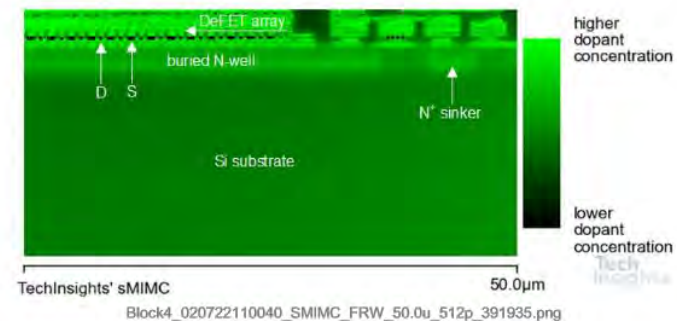
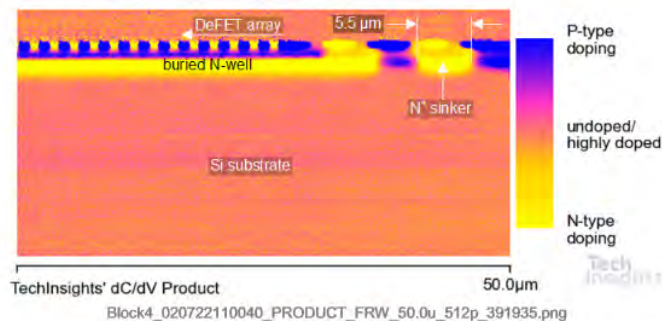
The Cirrus Logic Accused Products, and products incorporating them, include/Comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Cirrus Logic CLI1793B1 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing “DeFET Array,” an array of transistors each of which has active regions. Part of each active region is N-doped.

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transistors can be formed;

Power Block SPM/sMIM Analysis – Cross-Section

- The SPM/sMIM data shows a buried N-well layer (likely not epitaxially grown layers due to its non-uniformity on the Si substrate) formed on the Si substrate top. sMIM image on the right suggests that this layer is comprised of two sublayers, with the one closer to the Si substrate with a higher level of doping.
- The DeMOSFET layer is also made of sequences of S and D, with S characterized from its triple contacts (NiSi) on the sMIM image, whereas that of the drain is singular.
- Note that SCM imaging (such as the left image) is sensitive to the dopant type, with N-type material giving a negative (yellow) response, and P-type material giving a positive (purple) response.
- sMIM imaging (such as the right image) is sensitive to the dopant concentration level, with greater signal (brighter) corresponding to a higher dopant level, regardless of conductivity type.



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[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which

The Cirrus Logic Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the DeFET array shown in the SCM image reproduced at A-1 Claim 1, Element 2 shows multiple transistors with active regions.

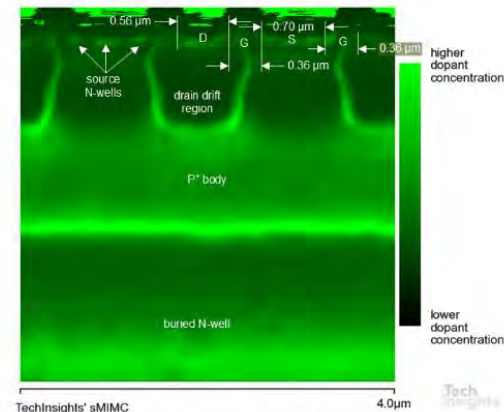
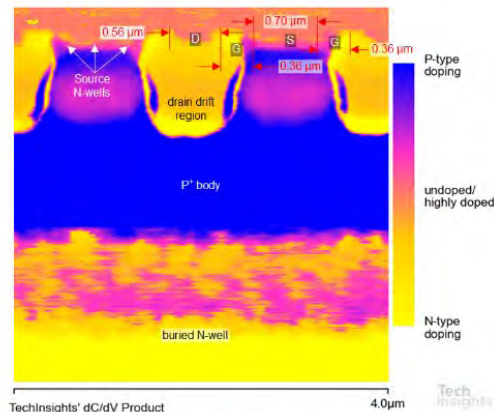
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

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| transistors can be formed; | |
| [Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and | The Cirrus Logic Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See</i> above at Preamble, Elements 2-3 (discussing “DeFET array”). |
| [Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at A-1 Claim 1, Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Cirrus Logic Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SPM images above show doping concentration and doping type as indicated in the legends to the right. The images below clearly show vertical dopant grading in the active regions surrounding the source, gate, and drain. |

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Power Block SPM/sMIM Analysis – Cross-Section

- Here one can (more) safely claim to see three source N-wells within the large P-well under the source. These are more obvious in the sMIM. The gates are on small P-doped wells, located closer to the source. These observations appear consistent with a DeMOSFET structure.



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2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

Upon information and belief, the substrate of the semiconductor device of the Cirrus Logic Accused Products is a p-type substance, as discussed above and shown in SPM/sMIM analysis.

5. The semiconductor device of claim 1, wherein the first active region and second active

The Cirrus Logic Accused Products meet this limitation. As shown above the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. See Tech Insights Report images reproduced above at Claim 1, Element 1.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

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| region contain one of either p-channel and n-channel devices. | |
| 6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant. | The Cirrus Logic Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in p-wells. The wells have graded dopants. <i>See</i> Tech Insights Report images reproduced above at Claim 1, Element 1 (annotating “wells”). |
| 7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region. | The accused products meet this limitation. <i>See, e.g.</i> , Tech Insights Report at 5 (“The logic and power blocks, both feature ... STI”). |
| 8. The semiconductor device of claim 1, | Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Cirrus Logic Accused Products. Cirrus Logic's website and its quality handbook refers to its use of focused ion beams. Cirrus Logic's recent patent applications also state that “[t]he circuit regions may be fabricated in the CMOS |

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

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| wherein the graded dopant is fabricated with an ion implantation process. | silicon substrate using standard processing techniques such as ion implantation..." Information about the fabrication process for the Cirrus Logic Accused Products, including usage of an ion implantation process, is in the possession of Defendants and is expected to be obtained through discovery. https://www.cirrus.com/company/quality/product-development/analysis/ https://www.cirrus.com/pubs/quality/Quality_Handbook_2021.pdf |
| [Claim 9, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include/comprise a semiconductor device. <i>See</i> above at Claim 1, Preamble. |
| [Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1. |
| [Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery. |

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

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| <p>[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.</p> |
| <p>[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4.</p> |
| <p>[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.</p> |

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

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| 10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 2. |
| 13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 5. |
| 14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 6. |

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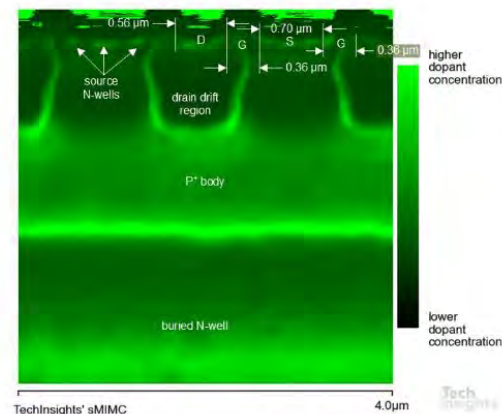
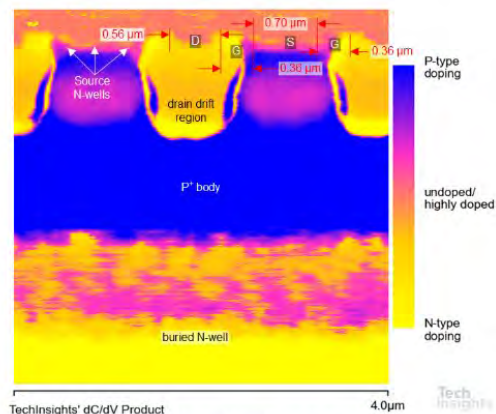
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| 15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region. | Upon information and belief, the Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 7. |
| 16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process. | Upon information and belief, the Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 8. |
| 17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2 and 3. |
| 18. The semiconductor device of claim 1, wherein the | The Cirrus Logic Accused Products meet this limitation. As discussed above for Claim 1, the Cirrus Logic Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery. |

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transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.

Power Block SPM/sMIM Analysis – Cross-Section

- Here one can (more) safely claim to see three source N-wells within the large P-well under the source. These are more obvious in the sMIM. The gates are on small P-doped wells, located closer to the source. These observations appear consistent with a DeMOSFET structure.



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Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

| U.S. Patent No. 10,734,481 | Exemplary Accused Product Cirrus Logic CLI1793B1 Power Management Integrated Circuit |
|--|---|
| [Claim 1, Preamble] A semiconductor device, comprising: | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble. This chart includes exemplary information regarding a representative example of the Cirrus Logic Accused Products, the Cirrus Logic CLI1793B1 PIMIC used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). The claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Cirrus Logic Accused Products, of which Cirrus Logic CLI1793B1 is one example, are semiconductor devices.</p> |
| [Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2. |

¹ https://www.cirrus.com/products/#psearch_T200² https://www.cirrus.com/products/#psearch_T100³ https://www.cirrus.com/products/#psearch_T400⁴ https://www.cirrus.com/products/#psearch_T300⁵ https://www.cirrus.com/products/#psearch_T800⁶ https://www.cirrus.com/products/#psearch_T3000

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| conductivity to the first doping type and within which transistors can be formed; | |
| [Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3. |
| [Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 6] at least one well region adjacent to | The Cirrus Logic Accused Products include a semiconductor device comprising at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. As shown by the following images obtained by SPM/sMIM analysis (<i>See</i> Exhibit A-1, Claim 1, Element 1), the images below clearly show blocks of highly |

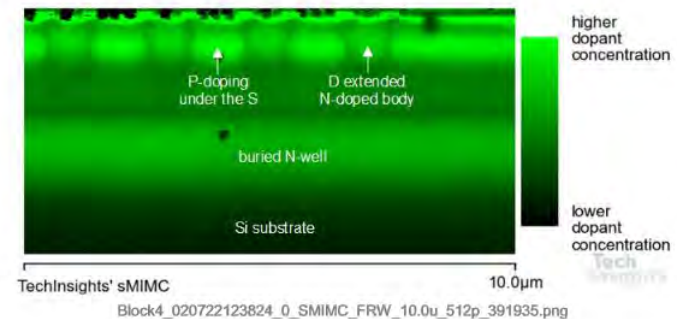
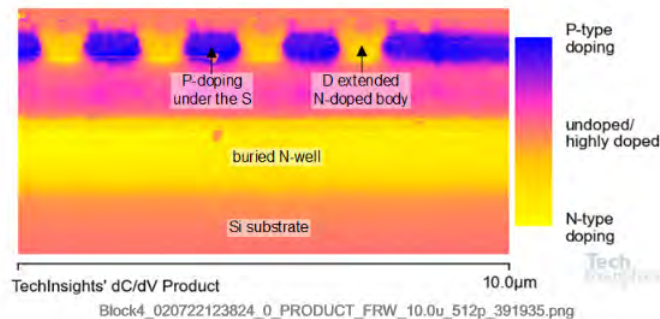
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

P-doped wells on top of a lightly P-doped layer. N-wells and p-wells in semiconductor devices often have a depth of about a few hundred nanometers, and at such depths a graded dopant concentration is present. *See also* SCM/SMIM analysis discussed at Exhibit A-1, Claim 1, Element 5 (showing carrier movement).

Power Block SPM/sMIM Analysis – Cross-Section

- The higher magnification SPM/sMIM images show a large N-doped block under the drain that is located farther from the gate, supportive of the DeMOSFET structure.
- Under the source, there are blocks of highly P-doped wells, which appear to be on top of a lightly P-doped layer. This P-doped layer is of course located on top of the buried N-well.



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2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

The Cirrus Logic Accused Products meet this limitation. *See* Exhibit A-1, Claim 2.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| 3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | Upon information and belief, the substrate of the Cirrus Logic Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Epitaxial layers are well known in the industry. <i>See</i> https://www.powerwaywafer.com/why-do-semiconductor-devices-need-epitaxial-layer.html . Additionally, Cirrus Logic has multiple patents disclosing epitaxial layers including U.S. Patent No. 5,786,622 and U.S. Patent Publication No. 2020/0006551. Because Cirrus Logic has patents disclosing this practice, and because it is well known in the art, the Cirrus Logic Accused Products likely meet this limitation. |
| 4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| one isolation region. | |
| 7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3. |
| 9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Cirrus Logic Accused Products meet this limitation. As shown by the images obtained by SPM/sMIM analysis (<i>See</i> above, Claim 1, Element 6), the Cirrus Logic Accused Products show blocks of highly P-doped wells on top of a lightly P-doped layer. |
| 13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 18. |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| source, a drain, a gate and a channel. | |
| 15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS). |
| 17. The semiconductor device of claim 1, wherein the device is a logic device. | The Cirrus Logic Accused Products meet this limitation. The CLI1793B1 die is approximately 290 μm thick. It contains a large logic region towards its right area, whereas there are several regions occupied with (nearly identical, i.e., similar pitches and visual configurations) power blocks. <i>See</i> Exhibit A-1, Claim 1, Preamble. |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

Device Summary

- This report presents an analysis of the Cirrus Logic CL11793B1 die within the Apple 338S00817 that is a silicon-based power management integrated circuit (PMIC) die. The CL11793B1 die is housed in a wafer level package (WLP), 338S00817, designed by Cirrus Logic. The 338S00817 component was extracted from the main PCB of the Apple iPhone 13 Pro smartphone.
- The CL11793B1 die is approximately 290 μm thick. It contains a large logic region towards its right area, whereas there are several regions occupied with (nearly identical, i.e. similar pitches and visual configurations) power blocks.
- The logic and power blocks, both feature a two-layer passivation (with a significant variable thickness, 0.17-0.91 μm), six layers of metal interconnect (one aluminum (Al) top metal layer and six copper (Cu) metal layers), tungsten (W) contacts, STI, and silicided polysilicon gate transistors.
- The power transistors are a form of LDMOS, likely a drain extended MOSFET (DeMOSFET) structure, where there are three small N-wells under the source within a large, lightly P-doped body, narrow P-doping under the gate, and an extended block of N-doped body under the drain. The extended body under the drain appears to be made of lighter doping interior and highly N-doped walls.
- The silicon (Si) die features one buried N-well (approximately 1.8 μm) between the P-doped body on top and (lightly doped) Si substrate. The MOSFET die uses a two-layer passivation made of a ~ 0.5 μm SiN outer and ~ 0.5 μm SiO inner layer, silicon oxide (SiO) pre-metal dielectric (PMD) layers, and a SiO gate dielectric. The polysilicon gates are ~ 70 nm thick, topped with NiSi (~ 29 -32 nm), and a SiN contact etch stop layer (CESL; ~ 31 -33 nm).

| | |
|---------------------------|---|
| Manufacturer | Apple |
| Part number | 338S00817 |
| Type | PMIC |
| Date code | 2125 (week 25 of 2021) |
| Package type | Wafer level package (WLP) |
| Package markings | 338S00817 RDWBB1AO2125 TW NQJQL |
| Package dimensions | 3.7 mm \times 5.1 mm \times 0.5 mm thick |
| Die markings | CIRRUS LOGIC 2021 <logo> CL11793B1 B69 CS37L10R06 B0 |

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[Claim 20, Preamble] A semiconductor device, comprising:

To the extent the preamble is a limitation, the Cirrus Logic Accused Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.

[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;

The Cirrus Logic Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| <p>[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2.</p> |
| <p>[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3.</p> |
| <p>[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.</p> |
| <p>[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| dopant concentration to aid carrier movement from the surface to the substrate; and | |
| [Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 6. |
| 22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 24. The semiconductor device of claim 20, wherein the first active region and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5. |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| second active region contain at least one of either p-channel and n-channel devices. | |
| 25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above, Claim 9. |

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

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| 31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 18. |
| 34. The semiconductor device of claim 20, wherein the device is a logic device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above, Claim 17. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
|---|--|
| <p>[Claim 1, Preamble] A VLSI semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a VLSI semiconductor device. The Cirrus Logic CLI1793B1 power management integrated circuit ("PIMIC") ("CLI1793B1") discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery.</p> <p>This chart includes exemplary information regarding a representative example of the Cirrus Logic Accused Products, the Cirrus Logic CLI1793B1 PIMIC used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). The claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.</p> |

¹ https://www.cirrus.com/products/#psearch_T200

² https://www.cirrus.com/products/#psearch_T100

³ https://www.cirrus.com/products/#psearch_T400

⁴ https://www.cirrus.com/products/#psearch_T300

⁵ https://www.cirrus.com/products/#psearch_T800

⁶ https://www.cirrus.com/products/#psearch_T3000

Greenthread, LLC v. Cirrus Logic, Inc. et al.

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

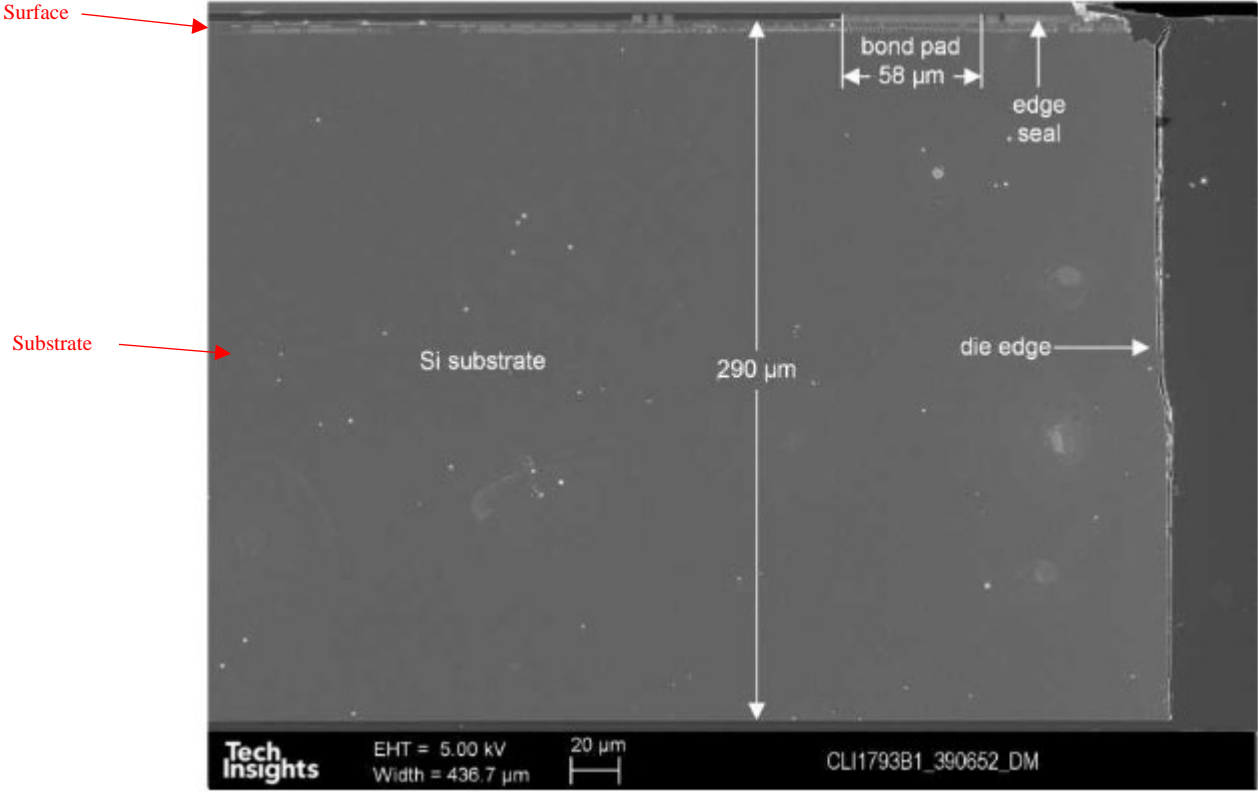
| U.S. Patent No. 11,121,222 | Accused Products |
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| |  <p>Surface</p> <p>Substrate</p> <p>Si substrate</p> <p>290 μm</p> <p>bond pad</p> <p>58 μm</p> <p>edge seal</p> <p>die edge</p> <p>Tech Insights</p> <p>EHT = 5.00 kV</p> <p>Width = 436.7 μm</p> <p>20 μm</p> <p>CLI1793B1_390652_DM</p> <p>Die Thickness_01_390652.png</p> |
| <p>[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.</p> |
| <p>[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.</p> |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| and within which transistors can be formed; | |
| [Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. <i>See</i> SPM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Cirrus Logic Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| 4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. <i>See</i> above at Claim 1, Element 6. |
| 5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3. |
| 9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| region are either p-type or n-type. | |
| 13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. <i>See</i> above at Claim 1, Element 6. |
| 15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15. |
| 17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors. | The Cirrus Logic Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. <i>See</i> above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Cirrus Logic Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. |
| 20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction. | The Cirrus Logic Accused Products meet this limitation. As shown by SEM imaging (<i>see</i> Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction. |
| [Claim 21, Preamble] A VLSI semiconductor device, comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble. |
| [Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1. |
| [Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof; | |
| [Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3. |
| [Claim 21, Element 4] transistors formed in at least one of the first active region or second active region; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. As shown by SPM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SPM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| 23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5. |
| 26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9. |
| 32. The VLSI semiconductor device of claim 21, wherein the | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| graded dopant is fabricated with an ion implantation process. | |
| 33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15. |
| 38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 20. |
| [Claim 39, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble. |
| [Claim 39, Element 1] a substrate of a first doping type at a first doping level; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2. |
| [Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3. |
| [Claim 39, Element 4] transistors formed in at least one | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| of the first active region or second active region; and | |
| [Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. |
| 40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. |
| [Claim 41, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble. |
| [Claim 41, Element 1] a substrate of a first doping type at a first doping level; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| [Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3. |
| [Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See</i> above at Claim 1, Element 5. <i>See</i> also SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 42, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble. |
| [Claim 42, Element 1] a substrate of a first doping type at a first doping level; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2. |
| [Claim 42, Element 3] a second active region separate from the first active region | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3. |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| disposed adjacent to the first active region and within which transistors can be formed; | |
| [Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region. | The Cirrus Logic Accused Products meet this limitation. SPM/sMIM analysis (see Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. <i>See</i> also SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 44, Preamble] A CMOS Semiconductor device comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a CMOS Semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18. |
| [Claim 44, Element 1]: a surface layer; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 1. |
| [Claim 44, Element 2] a substrate; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 44, Element 1. |
| [Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain). |

Exhibit A-3 to Greenthread's Complaint (U.S. Patent No. 11,121,222)

| U.S. Patent No. 11,121,222 | Accused Products |
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| <p>[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.</p> <p>Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants.</p> <p>Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-4 to Greenthread's Complaint (U.S. Patent No. 8,421,195)

| U.S. Patent No. 8,421,195 | Accused Products |
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| <p>[Claim 1, Preamble] A CMOS Semiconductor device comprising:</p> | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a VLSI semiconductor device. The Cirrus Logic CLI1793B1 power management integrated circuit ("PIMIC") ("CLI1793B1") discussed for claim 1 of Exhibit A-1 is a semiconductor device (see Exhibit A-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery.</p> <p>This chart includes exemplary information regarding a representative example of the Cirrus Logic Accused Products, the Cirrus Logic CLI1793B1 PIMIC used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). The claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a surface layer;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 1.</p> |
| <p>[Claim 1, Element 2] a substrate;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 2.</p> |
| <p>[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 3.</p> |
| <p>[Claim 1, Element 4] a single drift layer disposed between the other</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (<i>see</i> Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers</p> |

¹ https://www.cirrus.com/products/#psearch_T200

² https://www.cirrus.com/products/#psearch_T100

³ https://www.cirrus.com/products/#psearch_T400

⁴ https://www.cirrus.com/products/#psearch_T300

⁵ https://www.cirrus.com/products/#psearch_T800

⁶ https://www.cirrus.com/products/#psearch_T3000

Exhibit A-4 to Greenthread's Complaint (U.S. Patent No. 8,421,195)

| U.S. Patent No. 8,421,195 | Accused Products |
|---|--|
| surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and | from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implemented layer. | The Cirrus Logic Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implemented layer. |
| 3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer. |
| 5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5. |
| 6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5. |

Exhibit A-5 to Greenthread's Complaint (U.S. Patent No. 9,190,502)

| U.S. Patent No. 9,190,502 | Accused Products |
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| <p>[Claim 7, Preamble] A semiconductor device comprising:</p> | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products include a VLSI semiconductor device. The Cirrus Logic CLI1793B1 power management integrated circuit ("PIMIC") ("CLI1793B1") discussed for claim 1 of Exhibit A-1 is a semiconductor device (see Exhibit A-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery.</p> <p>This chart includes exemplary information regarding a representative example of the Cirrus Logic Accused Products, the Cirrus Logic CLI1793B1 PIMIC used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). The claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 7, Element 1] a surface layer;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 1.</p> |
| <p>[Claim 7, Element 2] a substrate;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 2.</p> |
| <p>[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 3.</p> |

¹ https://www.cirrus.com/products/#psearch_T200

² https://www.cirrus.com/products/#psearch_T100

³ https://www.cirrus.com/products/#psearch_T400

⁴ https://www.cirrus.com/products/#psearch_T300

⁵ https://www.cirrus.com/products/#psearch_T800

⁶ https://www.cirrus.com/products/#psearch_T3000

Greenthread, LLC v. Cirrus Logic, Inc. et al.

Exhibit A-5 to Greenthread's Complaint (U.S. Patent No. 9,190,502)

| U.S. Patent No. 9,190,502 | Accused Products |
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| <p>[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SPM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 5. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussedf at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.</p> | <p>The Cirrus Logic Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

| U.S. Patent No. 11,316,014 | Accused Products |
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| <p>[Claim 1, Preamble] An electronic system, the system comprising:</p> | <p>To the extent the preamble is a limitation, the Cirrus Logic Accused Products include an electronic system. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each Cirrus Logic Accused Product is an electronic system, because a PMIC is an electronic system.</p> <p>This chart includes exemplary information regarding a representative example of the Cirrus Logic Accused Products, the Cirrus Logic CLI1793B1 PIMIC used in the Apple 338S00817 of the Apple iPhone 13 Pro smartphone. The Cirrus Logic CLI1793B1 is representative of the Cirrus Logic Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Cirrus Logic Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other Cirrus Logic Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). The claimed invention would have application in numerous types of Cirrus Logic products, including amplifiers¹, decoder and encoder integrated circuits (ICs)², digital-to-analog converters³, analog-to-digital converters⁴, haptic drivers⁵, voice processor ICs⁶, and other ICs because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Cirrus Logic Accused Products contain similar features as the Cirrus Logic CLI1793B1, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Preamble.</p> |
| <p>[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 1.</p> |
| <p>[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.</p> |

¹ https://www.cirrus.com/products/#psearch_T200

² https://www.cirrus.com/products/#psearch_T100

³ https://www.cirrus.com/products/#psearch_T400

⁴ https://www.cirrus.com/products/#psearch_T300

⁵ https://www.cirrus.com/products/#psearch_T800

⁶ https://www.cirrus.com/products/#psearch_T3000

Greenthread, LLC v. Cirrus Logic, Inc. et al.

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

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| [Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3. |
| [Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 4. |
| [Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 5. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element 6. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5, 6. |
| 2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 2. |
| 3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a non-epitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 3. |
| 4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 4. |

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

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| logic formed by one of either p-channel and n-channel devices. | |
| 5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 5. |
| 6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 6. |
| 7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 7. |
| 8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 8. |
| 9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 9. |
| 13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 13. |
| 15. The system of Claim 1, wherein the at least one semiconductor | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 15. |

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

| | |
|---|--|
| device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | |
| 17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 17. |
| 20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 20. |
| [Claim 21, Preamble] An electronic system, the system comprising: | To the extent the preamble is a limitation, the Cirrus Logic Accused Products include an electronic system. <i>See</i> above at Claim 1, Preamble. |
| [Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including: | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1a. |
| [Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1b. |
| [Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2. |
| [Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3. |
| [Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region; | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1e. |
| [Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

| | |
|--|---|
| movement from the surface to an area of the substrate where there are no active regions; and | |
| [Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. <i>See also</i> SPM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 23. |
| 24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 24. |
| 25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 25. |
| 26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 26. |
| 27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 27. |

Exhibit A-6 to Greenthread's Complaint (U.S. Patent No. 11,316,014)

| | |
|---|---|
| region. | |
| 28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type. | The Cirrus Logic Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 28. |



techinsights.com

Apple/Cirrus Logic 338S00817 Power Management Integrated Circuit

Power Essentials Summary

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PEF-2110-802

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Overview

- This a Power Essentials (PEF) summary document, provided as a companion deliverable for Power Essentials projects. The complete PEF deliverable includes this document, which provides a summary of observed device metrics and salient features, the summary is supported by the following unannotated image folders:
 - Package optical photographs, package X-ray images, die photographs, optical photos of die feature image set
 - Plan-view images of the device delayed to the gate level
 - Exploratory cross-sectional scanning electron microscope (SEM) images of the device structure
 - Detailed cross-sectional scanning capacitance microscopy (SCM) and scanning microwave impedance microscopy (sMIM-C) analysis of the dopant structures
 - Detailed cross-sectional transmission electron microscope (TEM and STEM) images of the power device structure
 - Metal and dielectric layer composition identification based on TEM-EDS results
- The image set for a standard PEF project is derived from a beveled sample for SEM planar analysis, one plane of cross-sectioning for SEM structural analysis, a single TEM sample for the detailed structural analysis, and planar and cross-sectional SCM and sMIM analysis. Value added information, such as additional planes of cross-sectioning, may be included on a case-by-case basis.
- The Power Essentials deliverable provides basic competitive benchmarking information and enables cost-effective tracking of multiple competitors' technology.

Company Profile

- Apple Inc. was founded in 1976 in California, USA, originally as “Apple Computers”. Apple is heavily focused on manufacturing electronic devices such as computers, laptops, TVs, smartphones, and audio systems, and in-house development of software for all varieties of its products [1].
- Cirrus Logic, founded in 1984, was originally a “fabless” semiconductor model company, until the early 1990’s when they acquired Crystal Semiconductor, and became a leading supplier of PC graphics chips, audio converters and chips for magnetic storage products. Their products have been used in smartphones, tablets, truly wireless headsets, wearables, laptops and AR/VR headsets. Cirrus Logic further broadened its industry presence after acquiring Wolfson Microelectronics in August 2014 along with several other technology companies to expand their participation in audio and voice technology [2].



Device Summary

- This report presents an analysis of the Cirrus Logic CLI1793B1 die within the Apple 338S00817 that is a silicon-based power management integrated circuit (PMIC) die. The CLI1793B1 die is housed in a wafer level package (WLP), 338S00817, designed by Cirrus Logic. The 338S00817 component was extracted from the main PCB of the Apple iPhone 13 Pro smartphone.
- The CLI1793B1 die is approximately 290 μm thick. It contains a large logic region towards its right area, whereas there are several regions occupied with (nearly identical, i.e. similar pitches and visual configurations) power blocks.
- The logic and power blocks, both feature a two-layer passivation (with a significant variable thickness, 0.17-0.91 μm), six layers of metal interconnect (one aluminum (Al) top metal layer and six copper (Cu) metal layers), tungsten (W) contacts, STI, and silicided polysilicon gate transistors.
- The power transistors are a form of LDMOS, likely a drain extended MOSFET (DeMOSFET) structure, where there are three small N-wells under the source within a large, lightly P-doped body, narrow P-doping under the gate, and an extended block of N-doped body under the drain. The extended body under the drain appears to be made of lighter doping interior and highly N-doped walls.
- The silicon (Si) die features one buried N-well (approximately 1.8 μm) between the P-doped body on top and (lightly doped) Si substrate. The MOSFET die uses a two-layer passivation made of a ~ 0.5 μm SiN outer and ~ 0.5 μm SiO inner layer, silicon oxide (SiO) pre-metal dielectric (PMD) layers, and a SiO gate dielectric. The polysilicon gates are ~ 70 nm thick, topped with NiSi (~ 29 -32 nm), and a SiN contact etch stop layer (CESL; ~ 31 -33 nm).

| | |
|---------------------------|---|
| Manufacturer | Apple |
| Part number | 338S00817 |
| Type | PMIC |
| Date code | 2125 (week 25 of 2021) |
| Package type | Wafer level package (WLP) |
| Package markings | 338S00817 RDWBB1AO2125 TW NQjQL |
| Package dimensions | 3.7 mm \times 5.1 mm \times 0.5 mm thick |
| Die markings | CIRRUS LOGIC 2021 <logo> CLI1793B1 B69 CS37L10R06 B0 |

Critical Information – Logic Block

| | |
|--|---|
| Die designer | Cirrus Logic |
| Die name | CLI1793B1 |
| Die foundry | GlobalFoundries |
| Wafer size | Likely 300 mm |
| Die markings | CIRRUS LOGIC 2021 <logo> CLI1793B1 B69 CS37L10R06 B0 |
| Die markings date | 2021 |
| Die size (full die) | 3.70 mm × 5.07 mm |
| Die thickness | 279-290 µm |
| Process type | Likely BCD |
| Number of metal layers | 7 (1 Al, 6 Cu) |
| Number of poly layers | 1 |
| Minimum metal pitch | 0.18 µm |
| Minimum contacted gate pitch | 0.26 µm |
| Process generation | 55 nm |
| Features measured to determine process generation | Contacted gate and metal 1 pitch |

Critical Dimensions – Power Blocks

| Feature | Material Composition | Thickness (μm) |
|--------------------------------|--|-------------------------------------|
| Passivation | SiN (outer layer) SiO (inner layer) | Variable (0.17 – 0.91) |
| Source and gate contact metal | NiSi | – |
| Metal layers | M1-M6: Cu M7: Al | M1-M5: 0.21 M6: 0.89 M7: 2.85 |
| PMD | PMD1: SiO PMD2: SiO | 0.25 0.12 |
| Interlevel dielectric (ILD) | SiO-SiN | 0.034-0.036 |
| Gate electrode | Polysilicon | ~0.072 |
| Gate dielectric | SiO | 0.006 |
| Contact etch stop layer (CESL) | SiO | 0.033 |
| Buried N-well | Si | ~1.8 |
| Substrate overall | Si | 270 |

Horizontal Critical Dimensions – Power Blocks

| Feature | Dimension (μm) |
|----------------------------|----------------|
| MOSFET array pitch (G-D-G) | 0.93 |
| MOSFET array pitch (G-S-G) | 1.11 |
| Polysilicon gate | 0.36 |
| Source contact width | 0.70 |
| Drain contact width | 0.35 |
| N ⁺ sinker | ~5.5 |
| Edge seal | 28 |

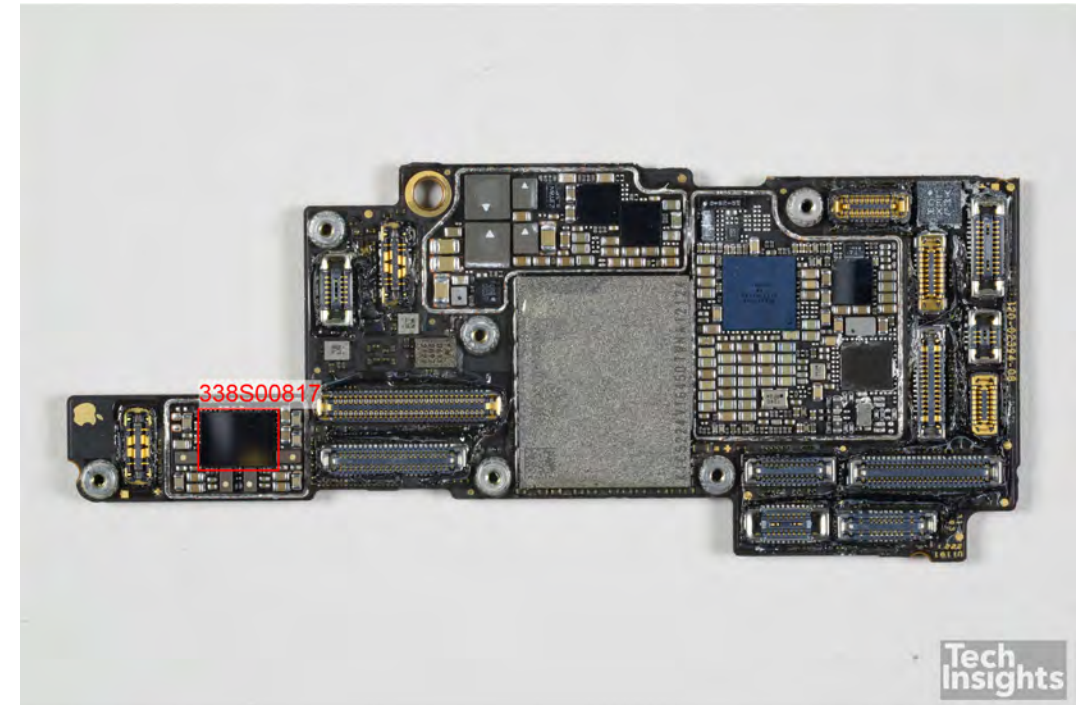
Package Analysis

Apple iPhone 13 Pro – Photograph & Main Printed Circuit Board

- The PMIC device component (338S00817) was extracted from the main PCB of the Apple iPhone 13 Pro smartphone, as outlined in the image below [\[3\]](#).



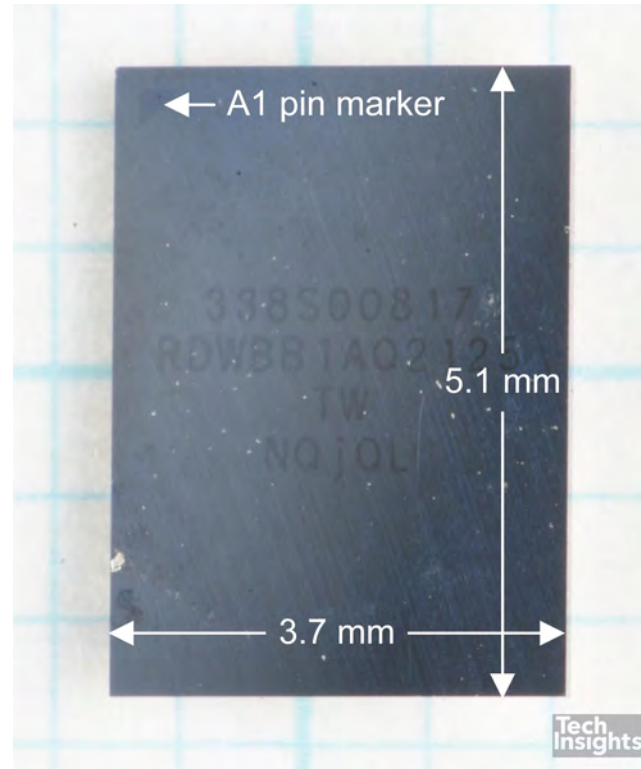
A2484_1E_Thumbnail.png



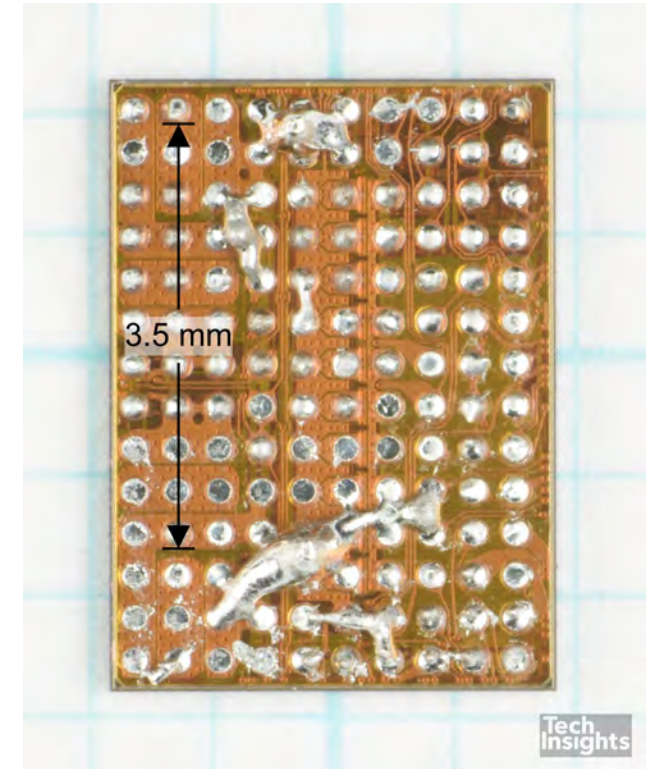
Img54447.png

338S00817 Package Photographs

- Wafer level package (WLP)
- 3.7 mm × 5.1 mm × 0.5 mm, including leads
- Solder ball pitch: 0.35 mm
- Package markings include:
 - 338S00817
 - RDWBB1AO2125
 - TW
 - NQjQL



338S00817_Pkg_Top_390325.png

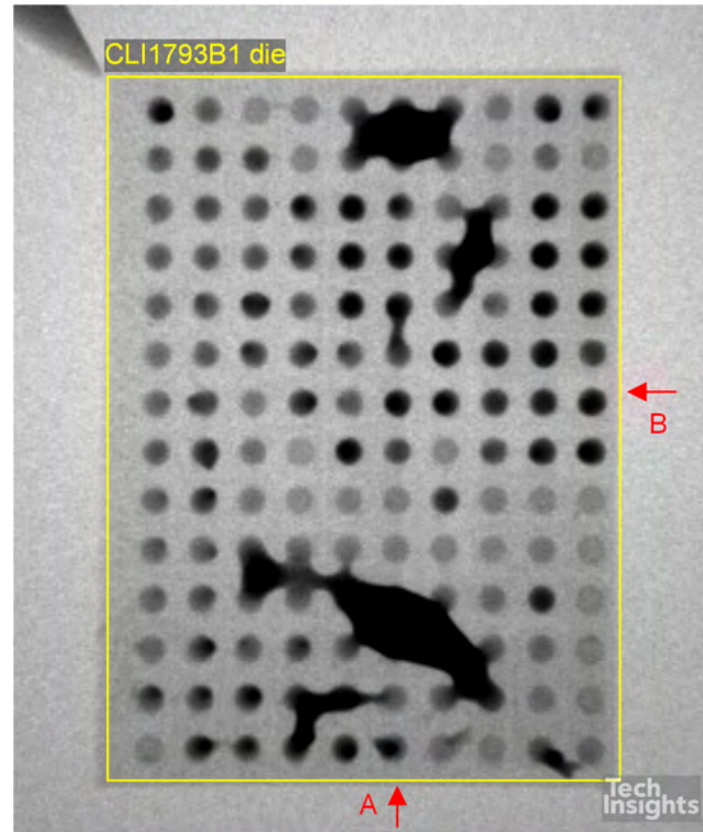
Top

338S00817_Pkg_Bot_390325.png

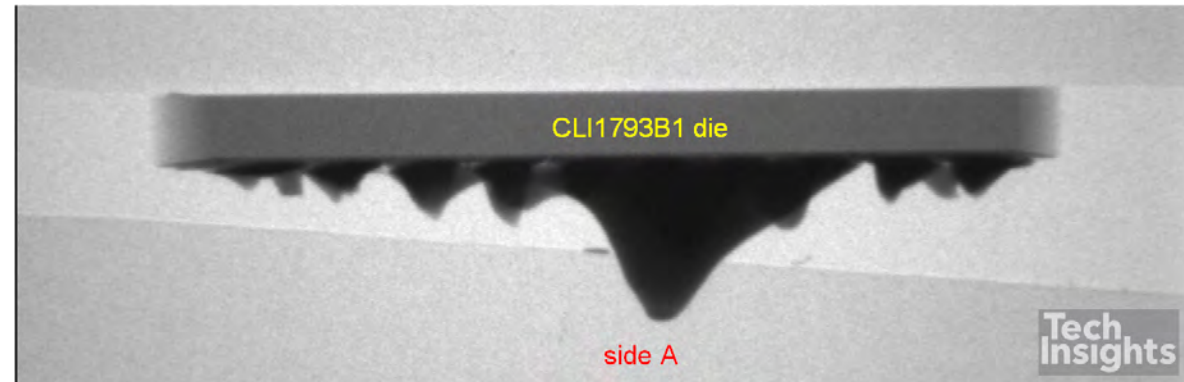
Bottom

338S00817 Package X-Rays

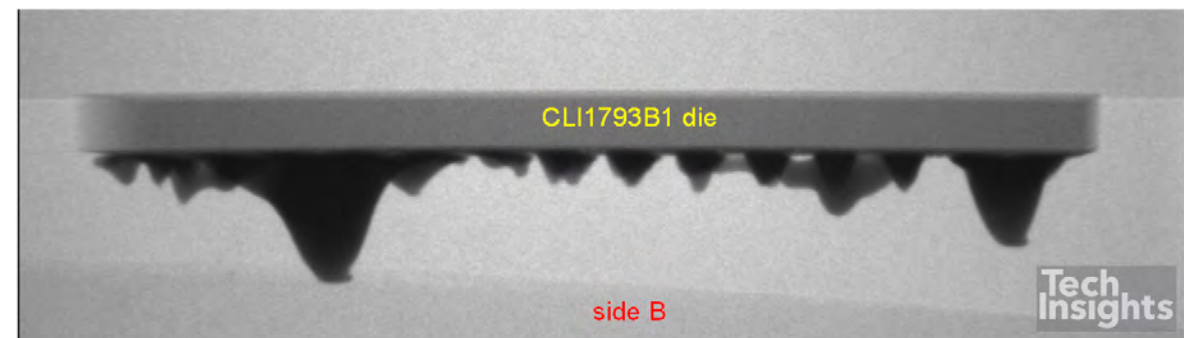
- The X-ray images suggest that the 338S00817 component uses a wafer level package (WLP) that houses a single die, occupying the entire available space of the package.



338S00817_XrayTop_390325.png



338S00817_XraySideA_390325.png

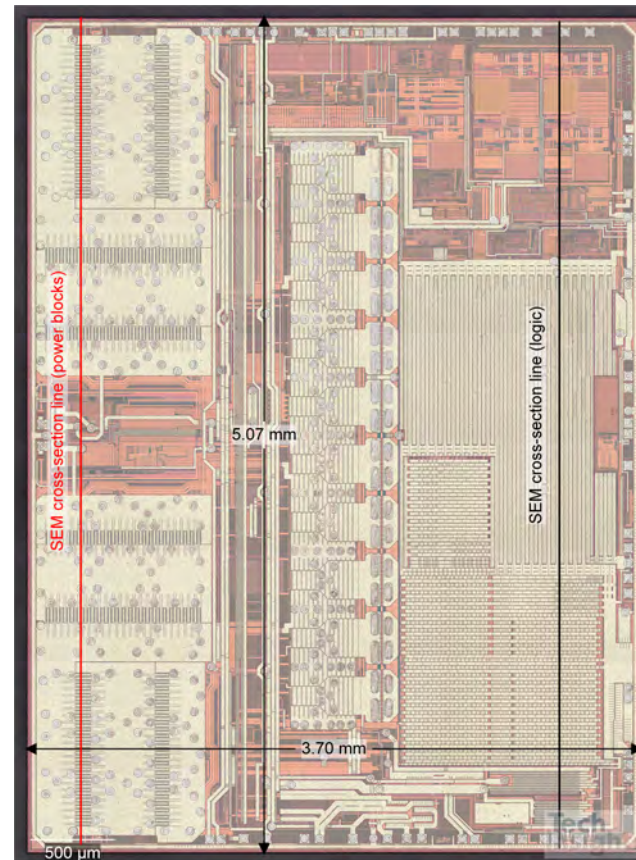


338S00817_XraySideB_390325.png

Die Optical Features

CLI1793B1 Die Photograph

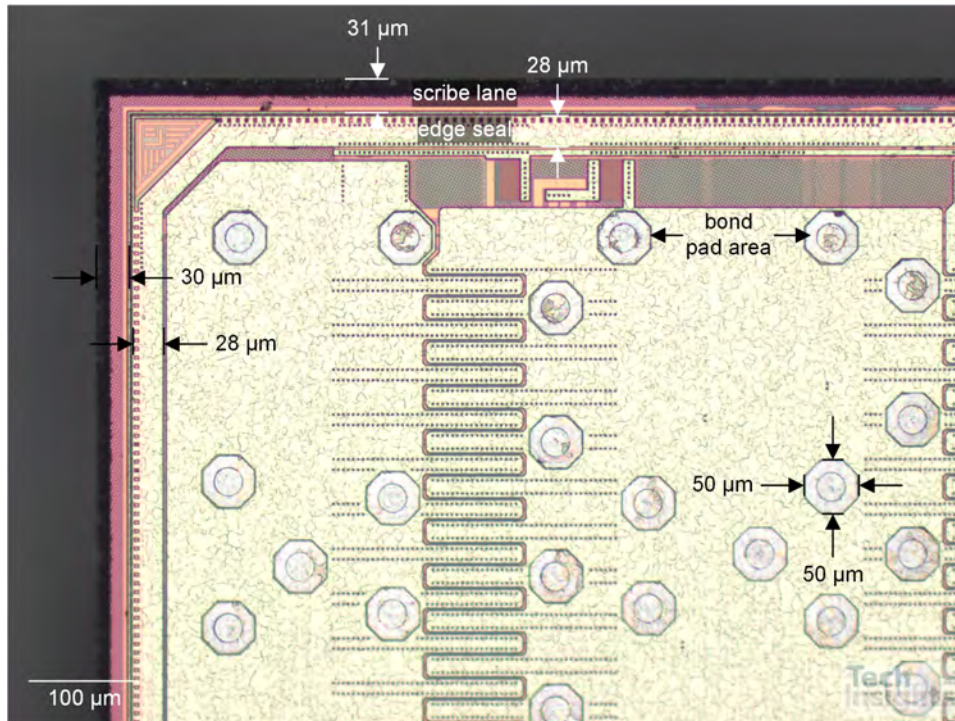
- Die size: 3.70 mm × 5.07 mm (18.76 mm²) (whole die). The die SEM and sMIM cross-section line is annotated.



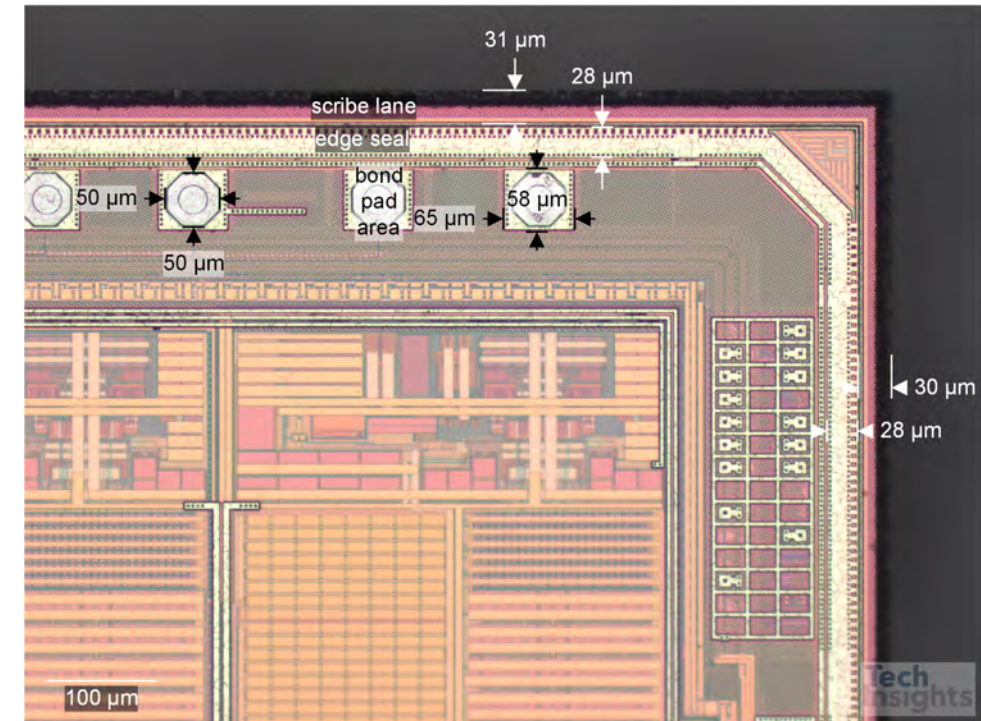
338S00817_CLI1793B1_390652_Oriented.png

CLI1793B1 Die Corners A and B

- The die's top left side (corner A – part of one of the power blocks) contains bond pads distributed throughout the area.
- Unlike in corner A, bond pads in the top right corner (B) are created within square-shaped bond pad areas. Bond pads are $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ on both sides.
- The scribe lane is $30\text{--}31\text{ }\mu\text{m}$ on the left, top, and right side. The edge seal is approximately $28\text{ }\mu\text{m}$.



338S00817_CLI1793B1_390652_DieCornerA.png

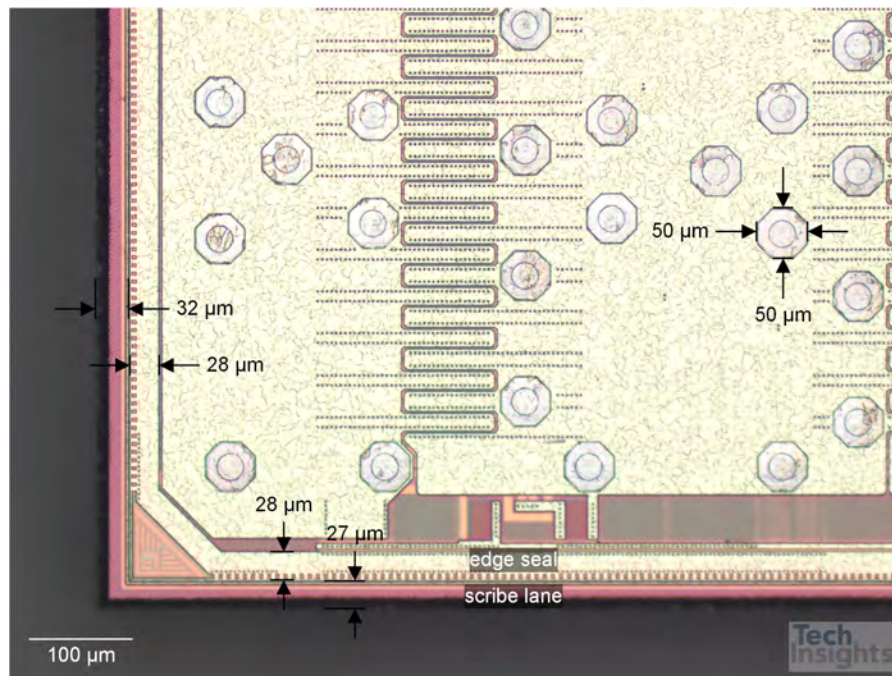
Corner A

338S00817_CLI1793B1_390652_DieCornerB.png

Corner B

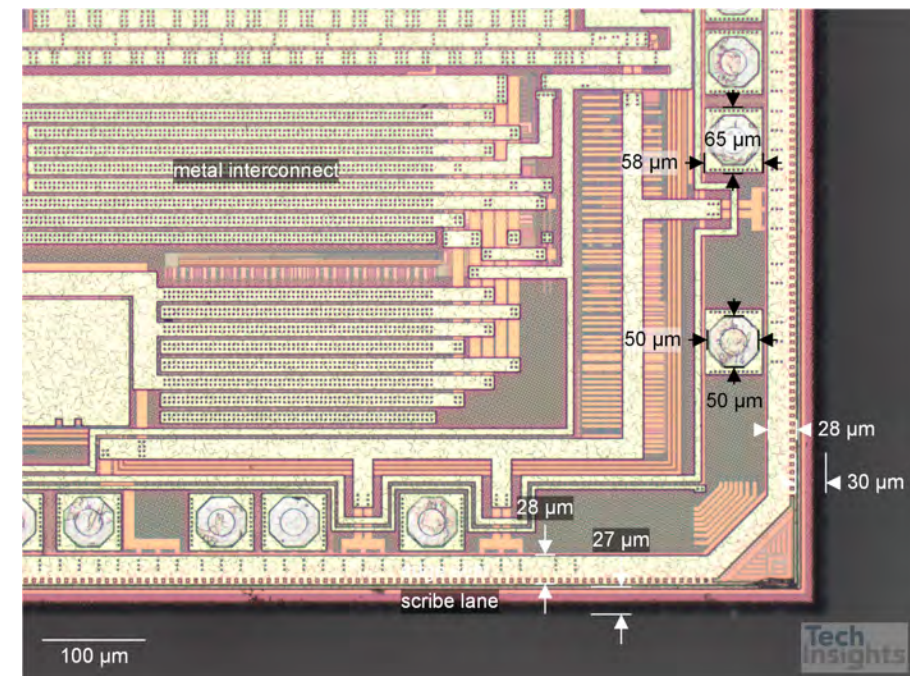
CLI1793B1 Die Corners C and D

- Similar to the top corners, bond pads on the power side (corner D) are created within square-shaped bond pad areas. Bond pads are $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ on both bottom corners.
- The scribe lane is $27\text{ }\mu\text{m}$ on the bottom side. The edge seal is $28\text{ }\mu\text{m}$ throughout the bottom side of the die.
- Metal interconnects can be seen on the bottom right side of the die (corner C).



338S00817_CLI1793B1_390652_DieCornerD.png

Corner D

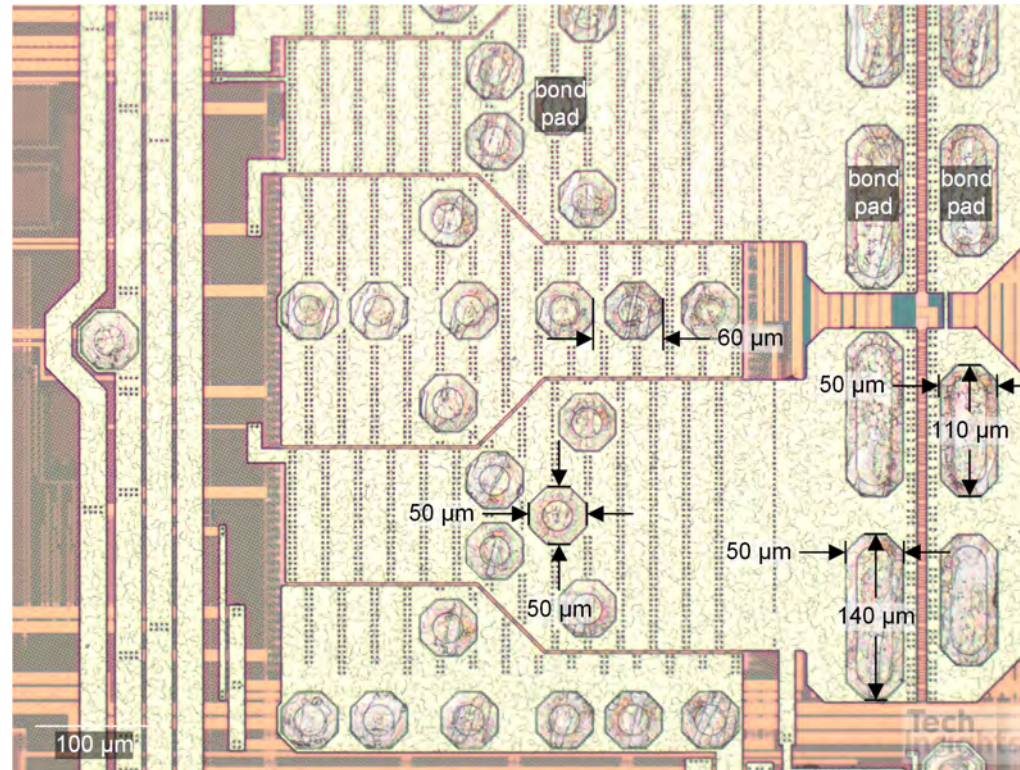


338S00817_CLI1793B1_390652_DieCornerC.png

Corner C

CLI1793B1 Die Power Block Contact Pads

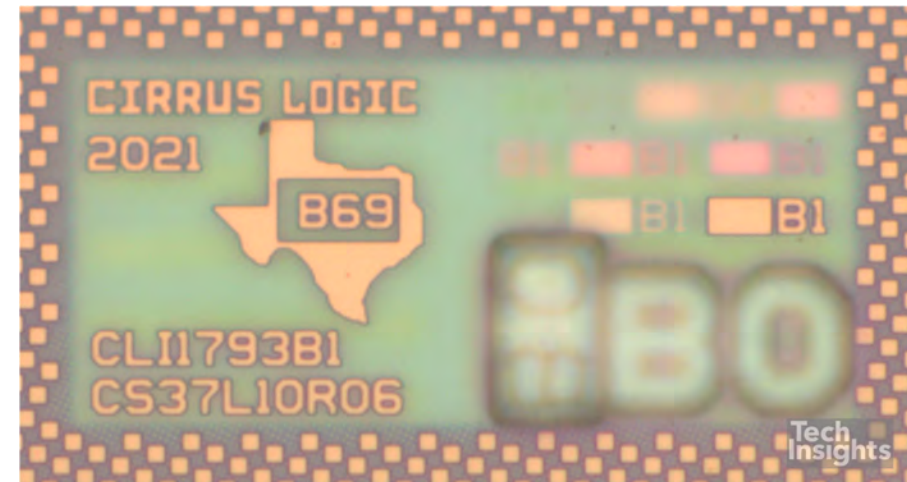
- Three sizes of bond pads can be seen, all with 50 μm width and with 50, 110, and 140 μm lengths.
- A minimum pitch of 60 μm can be approximated.



338S00817_CLI1793B1_390652_BondPads.png

CLI1793B1 Die Markings

- The die shows the following markings:
 - CIRRUS LOGIC
 - 2021 <logo>
 - CLI1793B1 B69
 - CS37L10R06 B0



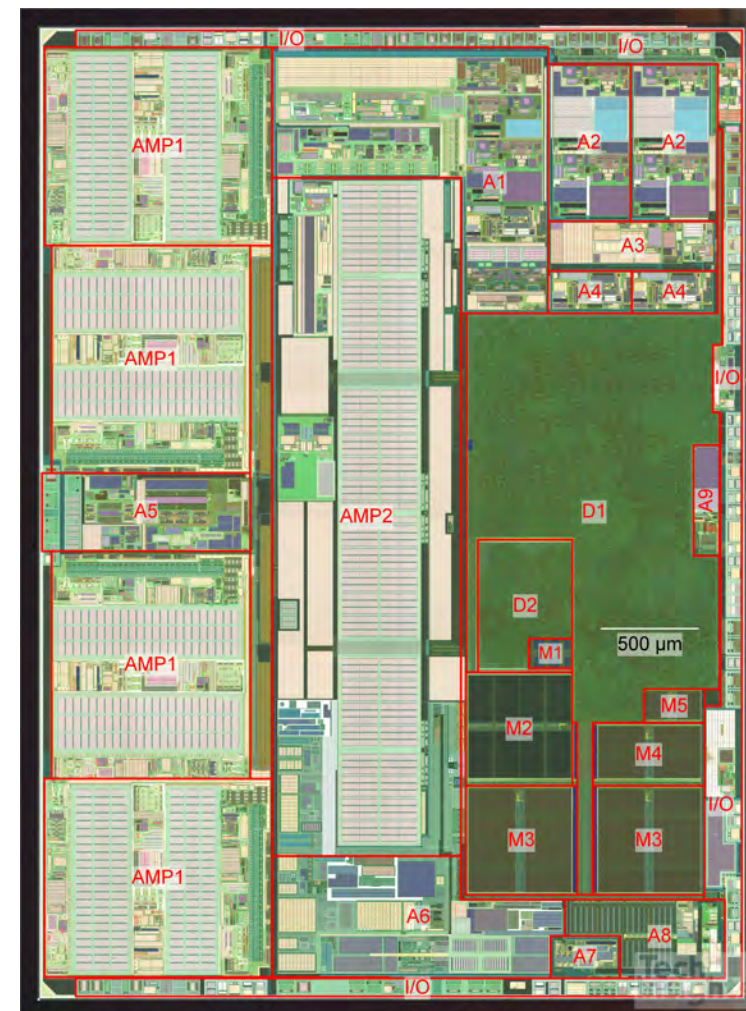
338S00817_CLI1793B1_390652_DieMrk-Rotated.png

Die Layout Planar Analysis

338S00817 Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

| Functional Description | Length (mm) | Width (mm) | Area (mm ²) | Percentage of Die |
|--|-------------|------------|-------------------------|-------------------|
| AMP1 (x4) - Likely power amplifier | 1.03 | 1.18 | 4.83 | 26.4 |
| AMP2 - Likely power amplifier | 3.51 | 0.98 | 3.42 | 18.7 |
| A1 – Likely bias generator for AMP2 | Irregular | | 1.28 | 7.0 |
| A2 (x2) - Unknown analog interface | 0.69 | 4.0 | 0.69 | 4.0 |
| A3 – Unknown analog likely bias/voltage generator | 0.26 | 0.88 | 0.23 | 1.2 |
| A4 - Unknown analog interface | 0.19 | 1.0 | 0.19 | 1.0 |
| A5 – Likely bias generator for AMP1 | 0.40 | 1.08 | 0.43 | 2.4 |
| A6 – Likely bias generator for AMP2 | Irregular | | 0.82 | 4.5 |
| A7 - Unknown analog | 0.22 | 0.36 | 0.08 | 0.4 |
| A8 - Unknown analog, looks like a fuse circuit or charge pumps | Irregular | | 0.27 | 1.5 |
| A9 – Likely clock generator | 0.13 | 0.57 | 0.08 | 0.4 |
| D1 – Logic core | Irregular | | 2.23 | 12.2 |
| D2 – Logic core | Irregular | | 0.30 | 1.6 |
| M1 – SRAM | 0.15 | 0.23 | 0.03 | 0.2 |
| M2 – SRAM | 0.59 | 0.55 | 0.32 | 1.8 |
| M3 (x2) – SRAM | 0.56 | 0.58 | 0.65 | 3.6 |
| M4 – SRAM | 0.33 | 0.58 | 0.19 | 1.0 |
| M5 – SRAM | 0.18 | 0.31 | 0.05 | 0.3 |
| IO – General purpose I/Os and ESDs | Irregular | | 1.32 | 7.2 |
| Total die utilization | | | 17.41 | 95.4 |
| Others | | | 0.88 | 4.6 |
| Total die | 5.01 | 3.65 | 18.29 | 100.0 |

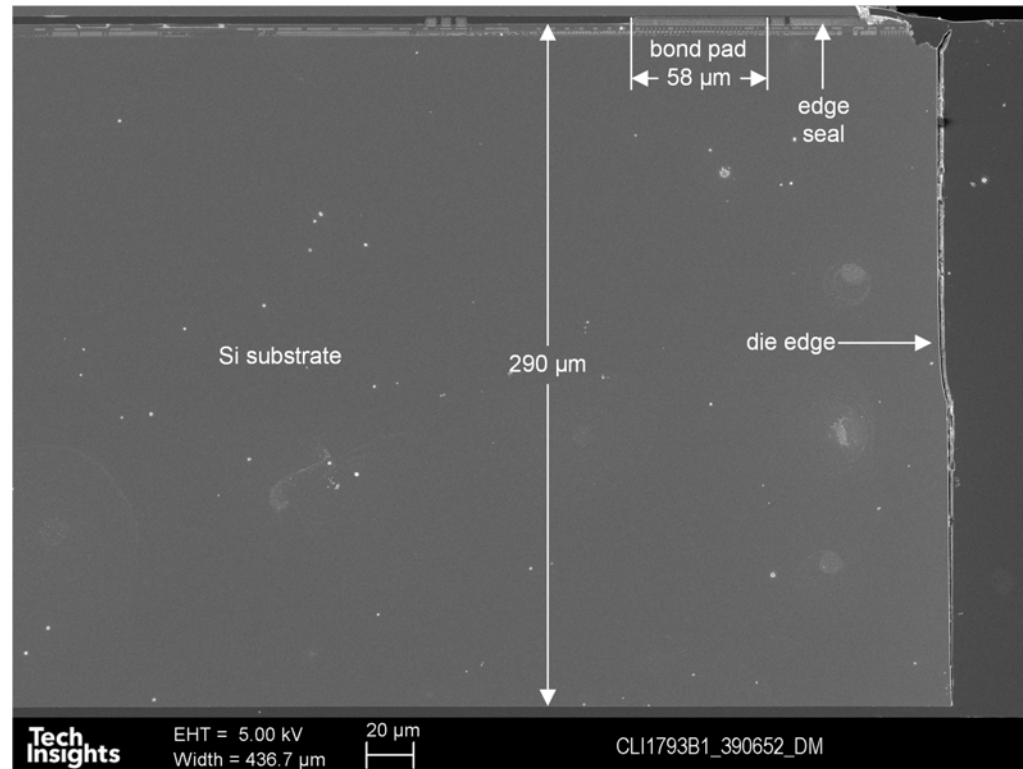


338S00817_CLI1793B_391547_BPoly.png

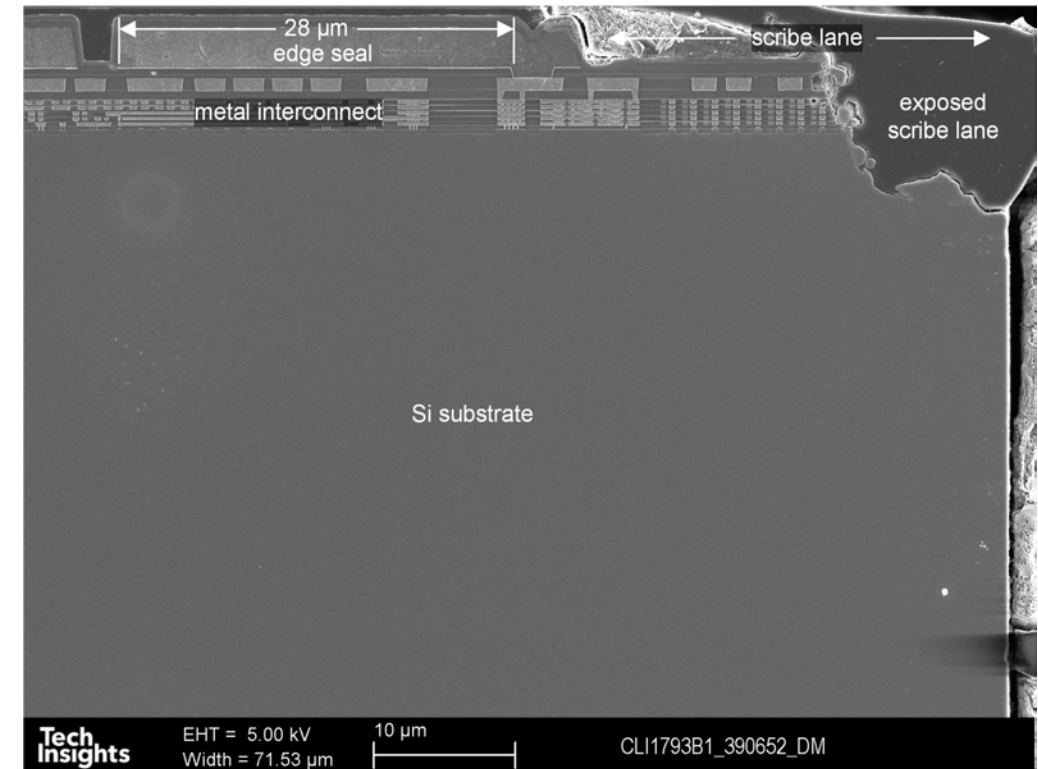
Die Cross-Sectional Analysis – Logic Area

Die Edge Overview – SEM Cross-Section

- The die's thickness in the logic region is 290 μm .
- The edge seal (that also maintains the same thickness throughout the die) is 28 μm wide.



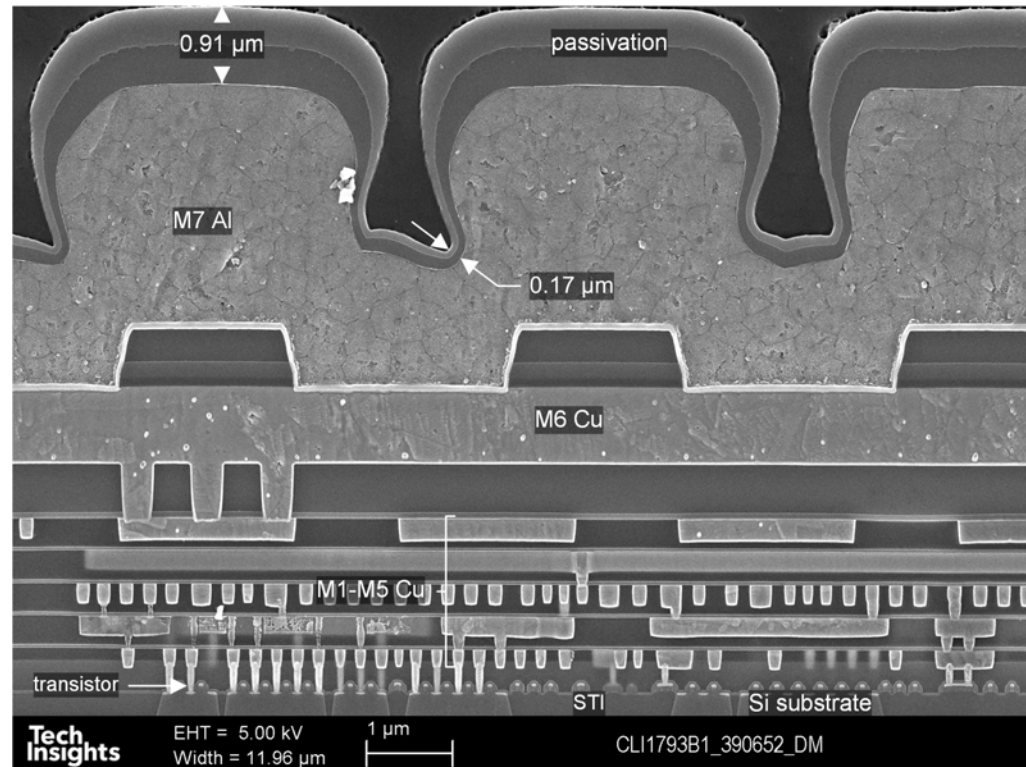
Die Thickness_01_390652.png



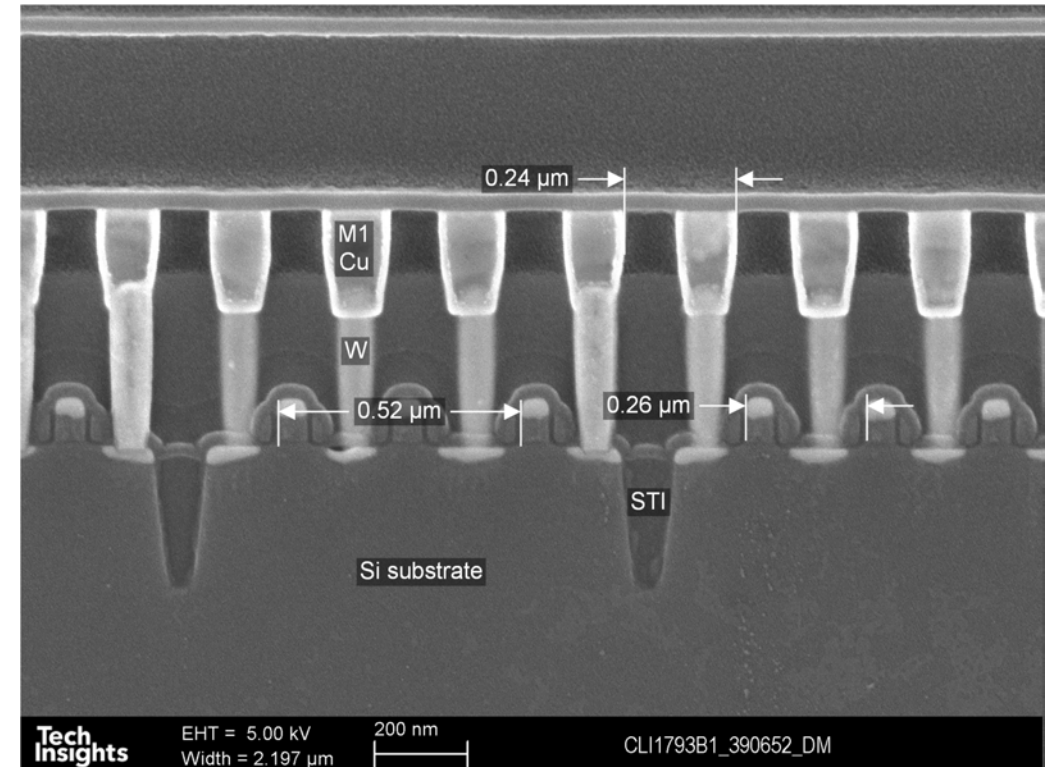
Die Edge_02_390652.png

General View and Transistors – SEM Cross-Section

- The die over the logic area features two-layer passivation (with a significantly variable thickness, 0.17-0.91 μm), seven layers of metal interconnect (one Al top metal layer and six Cu metal layers), W contacts, STI, and silicided polysilicon gate transistors.
- One can approximate a 0.26 μm (single and averaged) minimum contacted gate pitch.



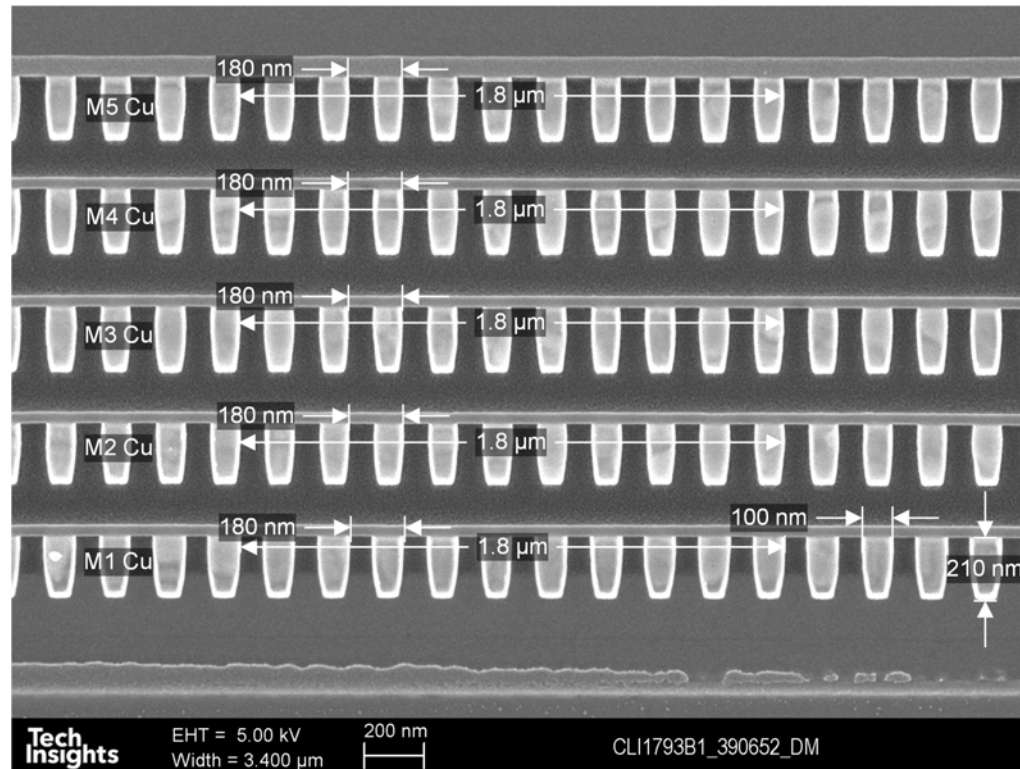
Transistors_37_390652.png



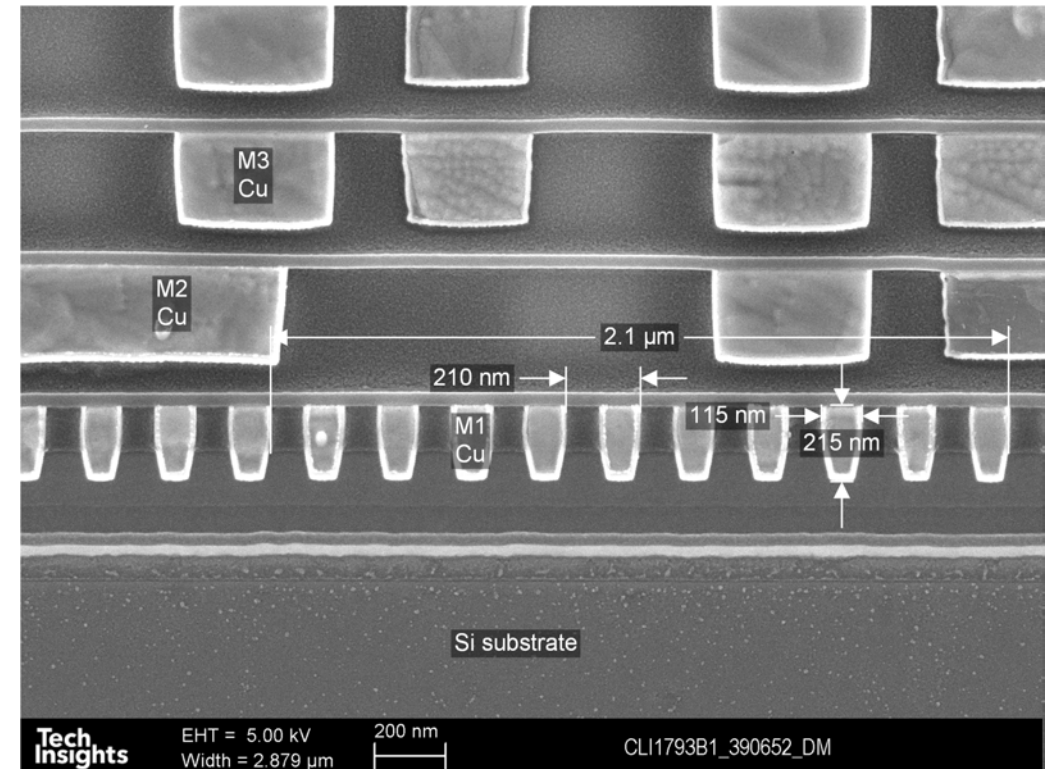
Transistors_44_390652.png

Metal Interconnect – SEM Cross-Section

- Minimum metal pitch is 0.18 μm , identical for metal layers one through five.
- Minimum metal width and thickness are 100 and 210 μm , respectively.



Lower Metal Stack_18_390652.png



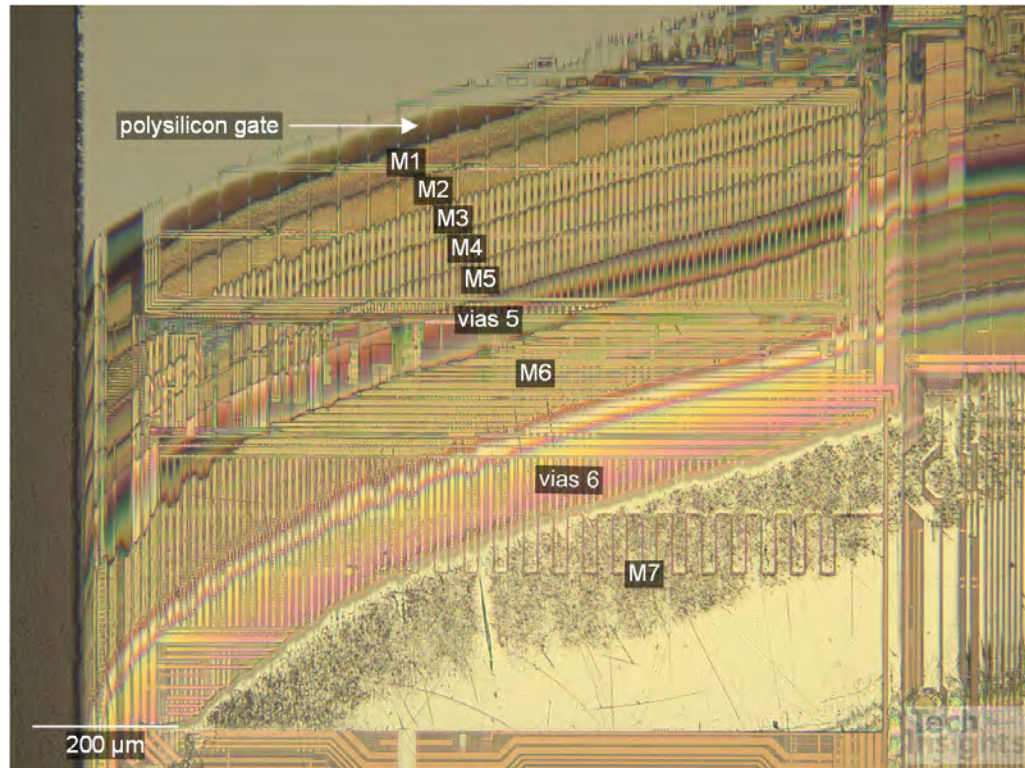
Metal 1_13_390652.png

Die Cross-Sectional Analysis – Power Block

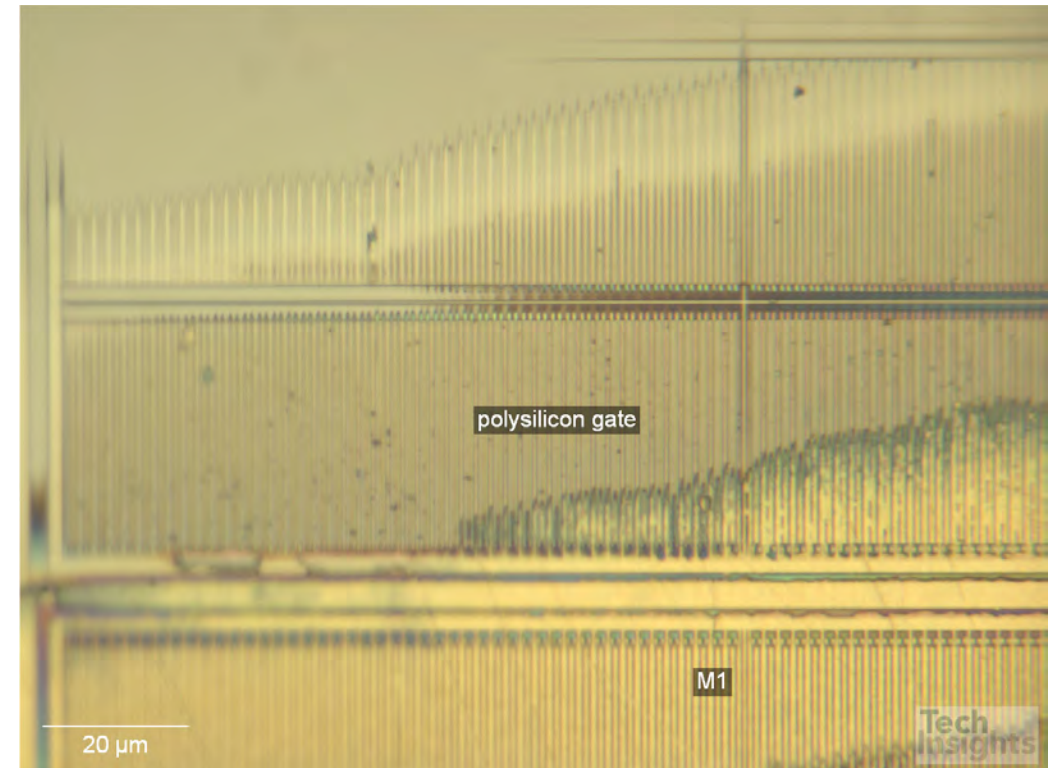
Part 1. Optical & SEM

Power Block (AMP1) – Gate Level Optical

- The optical images of the beveled die over the power block shows the seven metal layers. It is noteworthy that metal layers 3, 4, and 5 have identical directions.
- Polysilicon gates are arranged of closed loops throughout the power blocks.



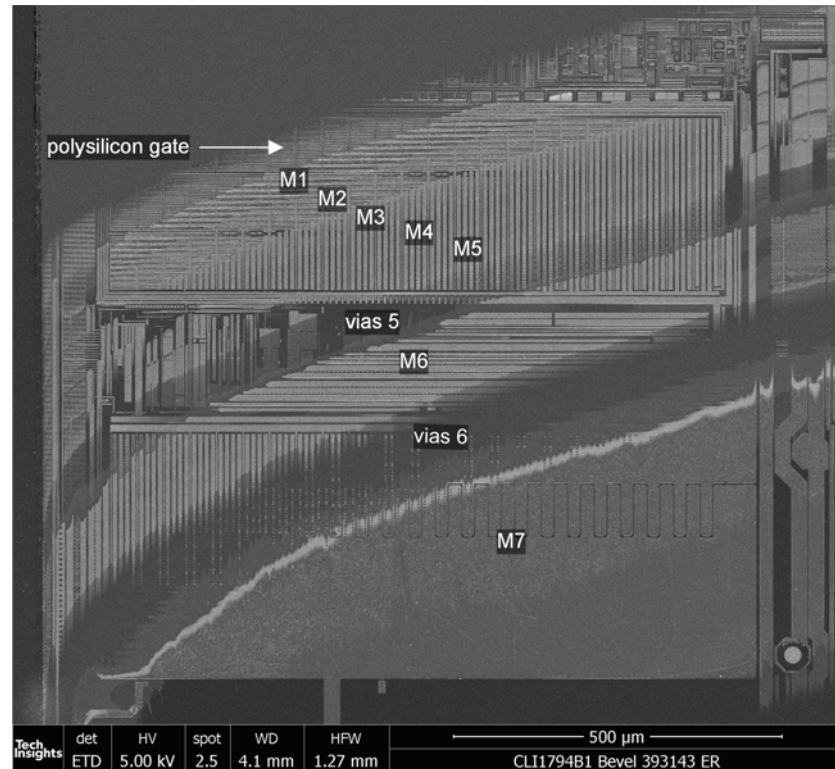
153_Block-3-4_393143_10x1r.png



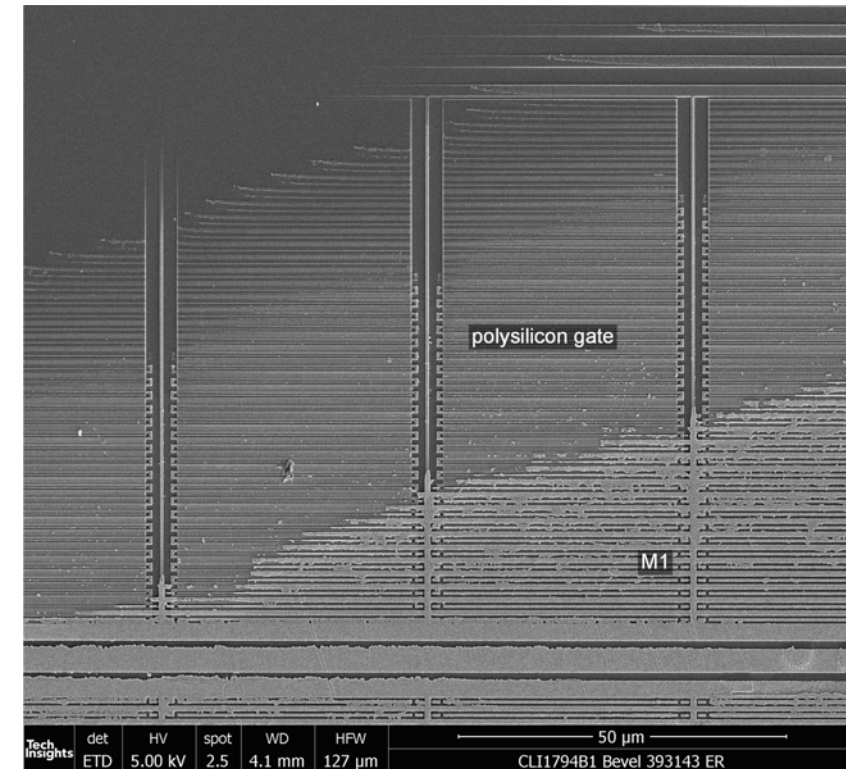
160_Block-9_393143_100x1r.png

Power Block (AMP1) – Gate Level SEM

- The SEM images of the beveled die over the power block shows the seven metal layers. It is noteworthy that metal layers 3, 4, and 5 have identical directions.
- Polysilicon gates are arranged of closed loops throughout the power blocks.



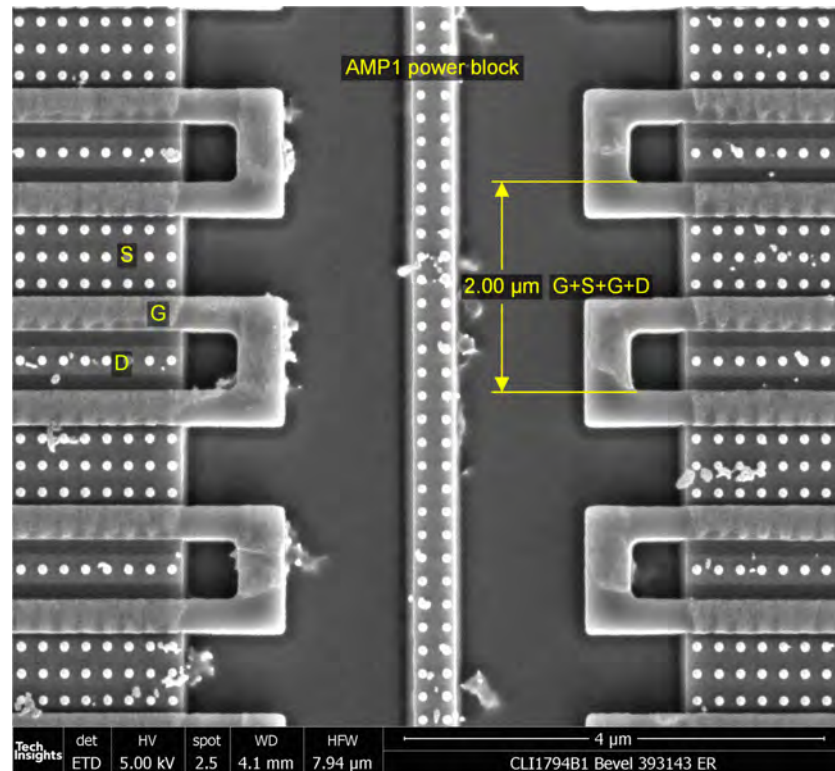
307_Blocks-3-4_100x_393143.png



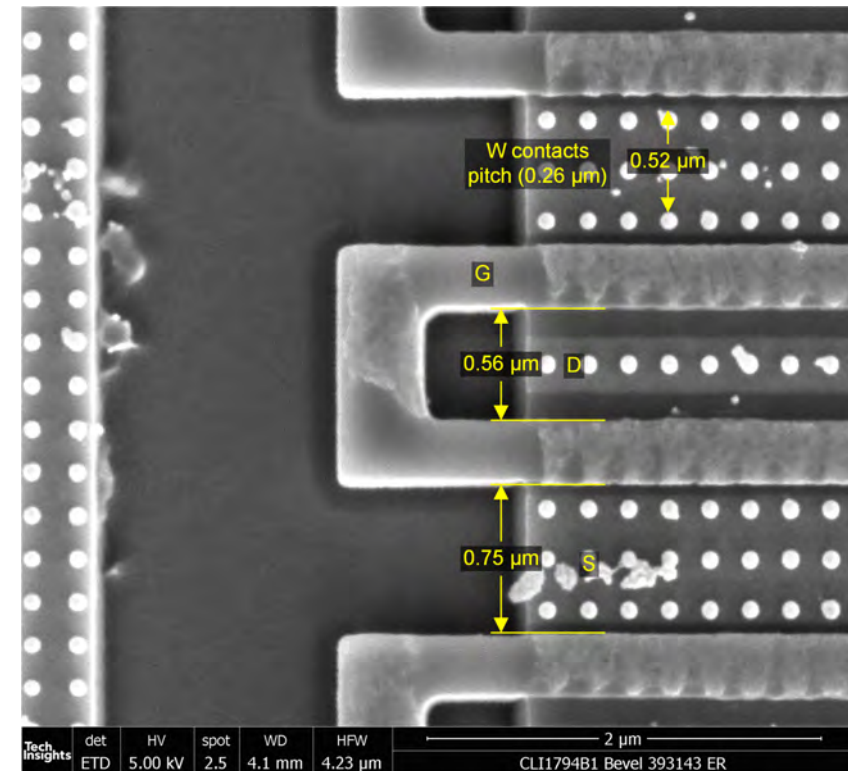
303_Block-3_1K_393143.png

Power Block (AMP1) – Gate Level SEM Details

- Gates on the power block show as closed-loop structures wrapping around the drain, where each loop is separated from the next with the source. The gate band is closer to the source, which is characterized with its triple contact connections. Drain has one single contact.
- Gate to gate distance is 0.75 and 0.56 μm with source and drain in between, respectively.



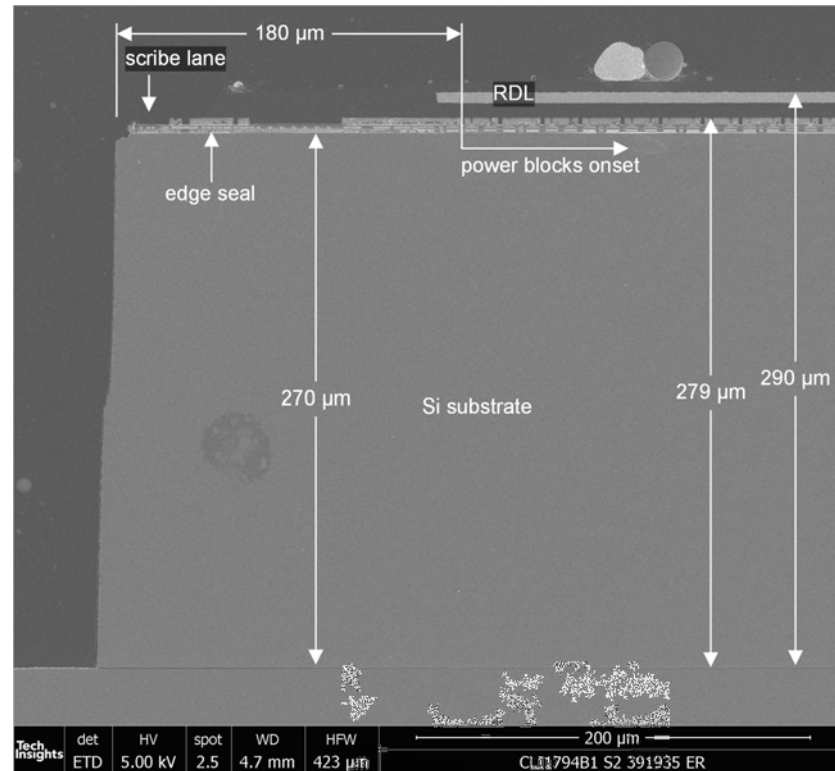
304_Block-3_16K_393143.png



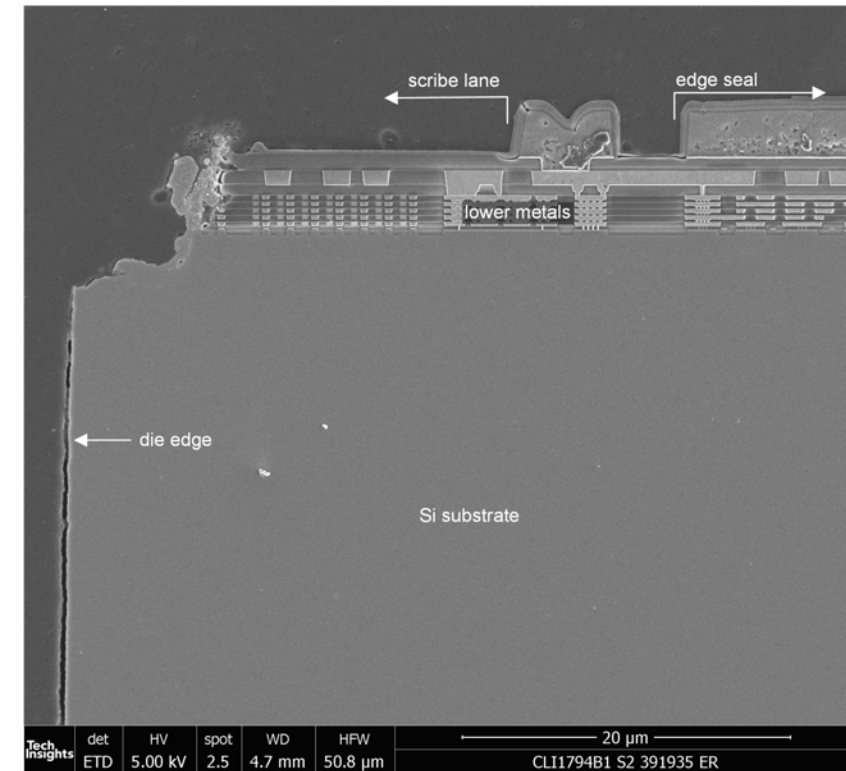
305_Block-3_30K_393143.png

Die Edge Overview – SEM Cross-Section

- The die's thickness in the power block's region is 279 μm to the top of the metal layers (290 μm including the RDL).
- Power blocks onset has an approximately 180 μm distance to the edge of the die.



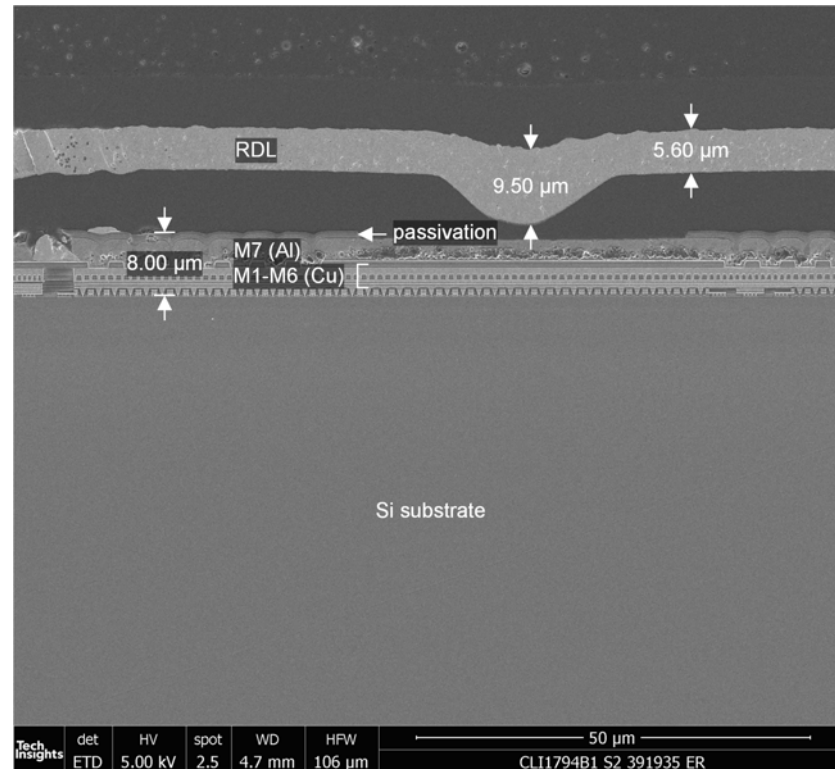
201_Die_Edge_Die_Thickness_300x_391935.png



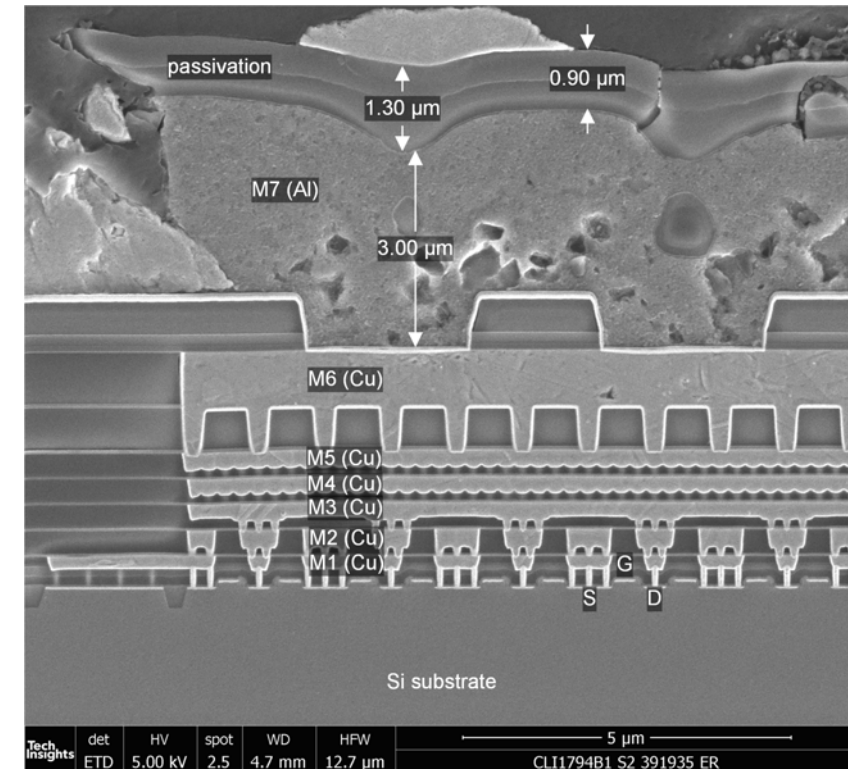
203_Die_Edge_Die_Seal_2p5K_391935.png

General Structure of Power Array – SEM Cross-Section

- The power block side of the die comprises seven metal interconnect layers, one top Al and six Cu layers. Transistors and metal interconnect layers have a (average) collective thickness of $\sim 8\text{ }\mu\text{m}$.
- A dual layer passivation (thickness of 0.90 to $1.30\text{ }\mu\text{m}$) is noticeable on the Al metal layer ($\sim 3\text{ }\mu\text{m}$).



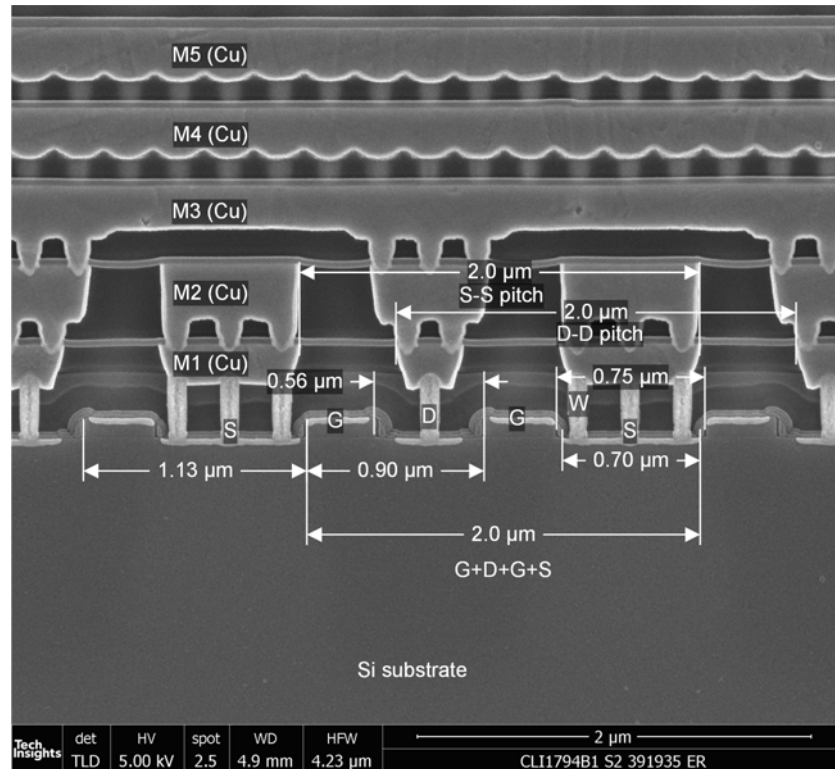
213_Block-03_Array_1p2K_391935.png



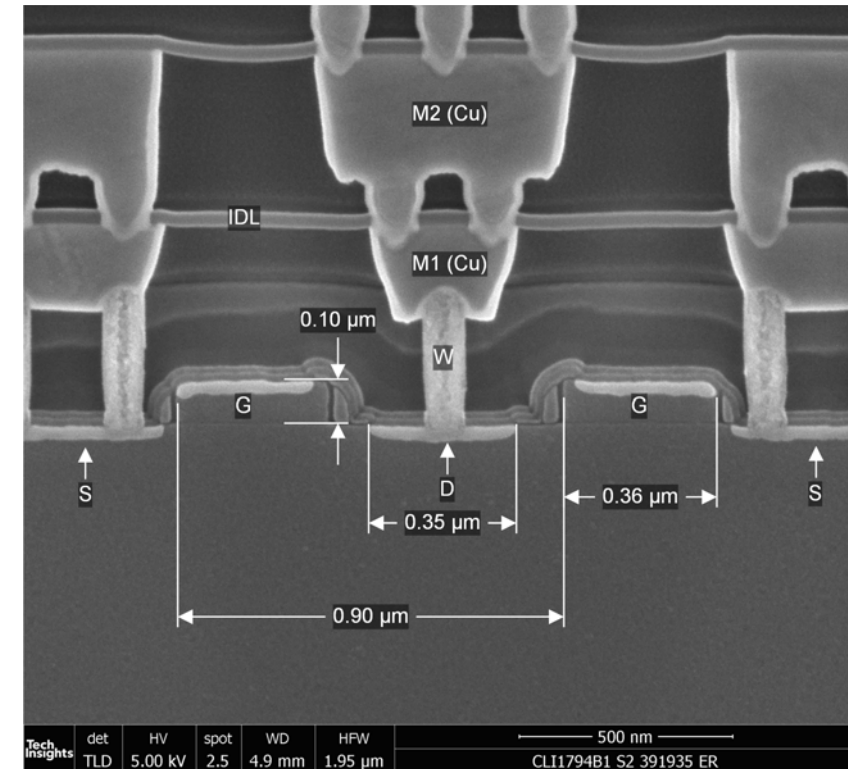
214_Block-03_Array_Edge_10K_391935.png

Power Transistors – SEM Cross-Section

- A minimum contacted gate pitch of 0.90 μm is observed. Drain to drain and source to source pitches are identically 2.04 μm .
- Source and drain metal contacts have 0.35 and 0.70 μm widths, respectively.
- Gate width and thickness are 0.36 and 0.10 μm , respectively.



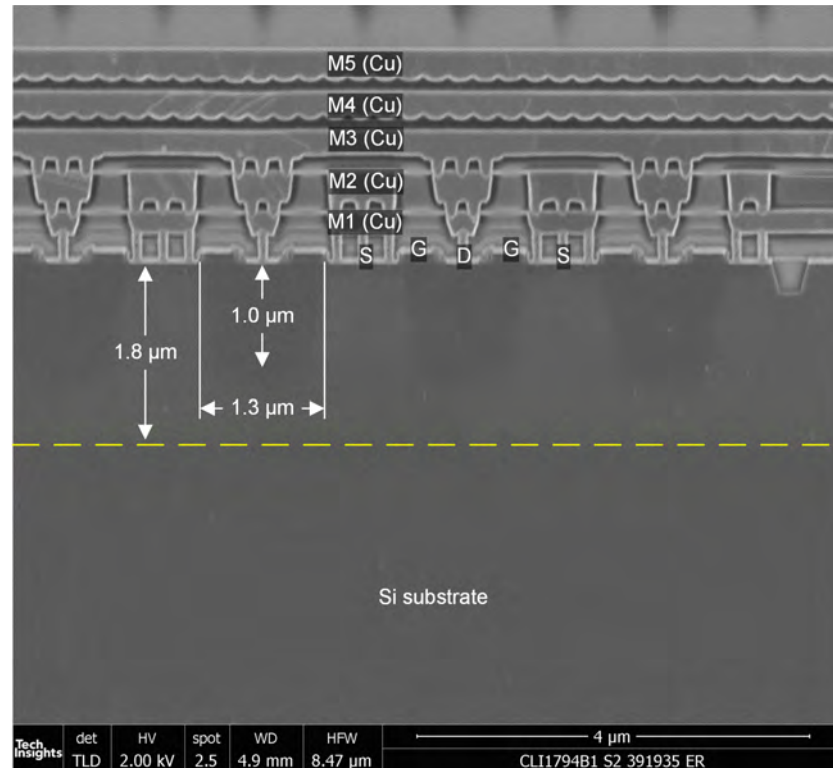
248_Block-6_Gates_30K_391935.png



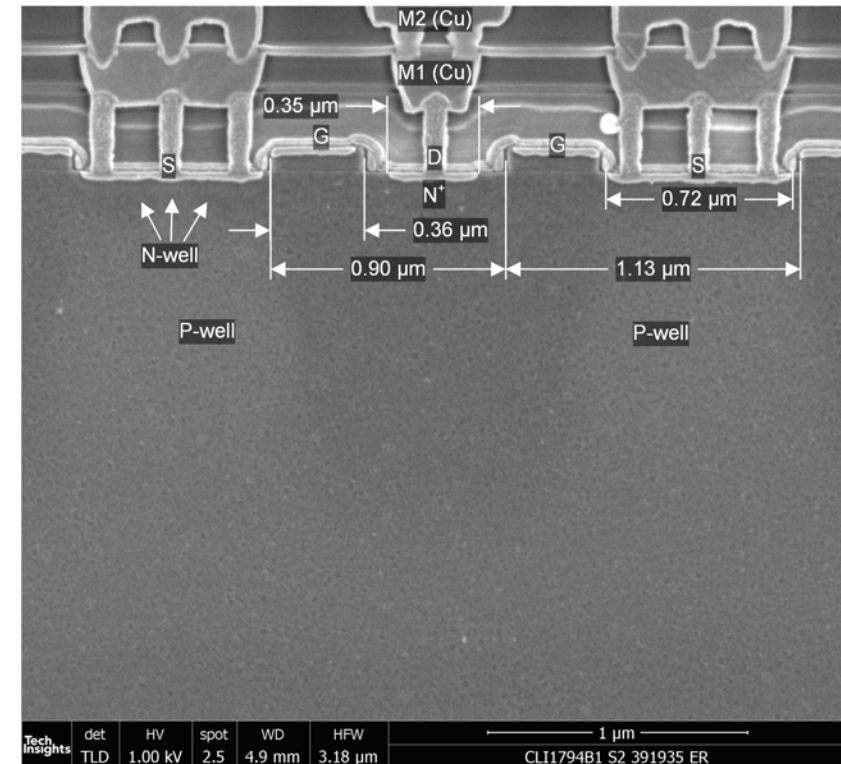
249_Block-6_Gates_65K_391935.png

Power Transistors (LVSEM) – SEM Cross-Section

- Low voltage SEM (typically taken at 1-5 kV to reveal surface features) images show N-wells with a thickness of $1.0\ \mu\text{m}$ and maximum width of $1.3\ \mu\text{m}$ within a P-well body, on top of the main Si substrate.
- Thickness (distance between top of the Si substrate and S/D contacts) of the P-well is about $1.8\ \mu\text{m}$.



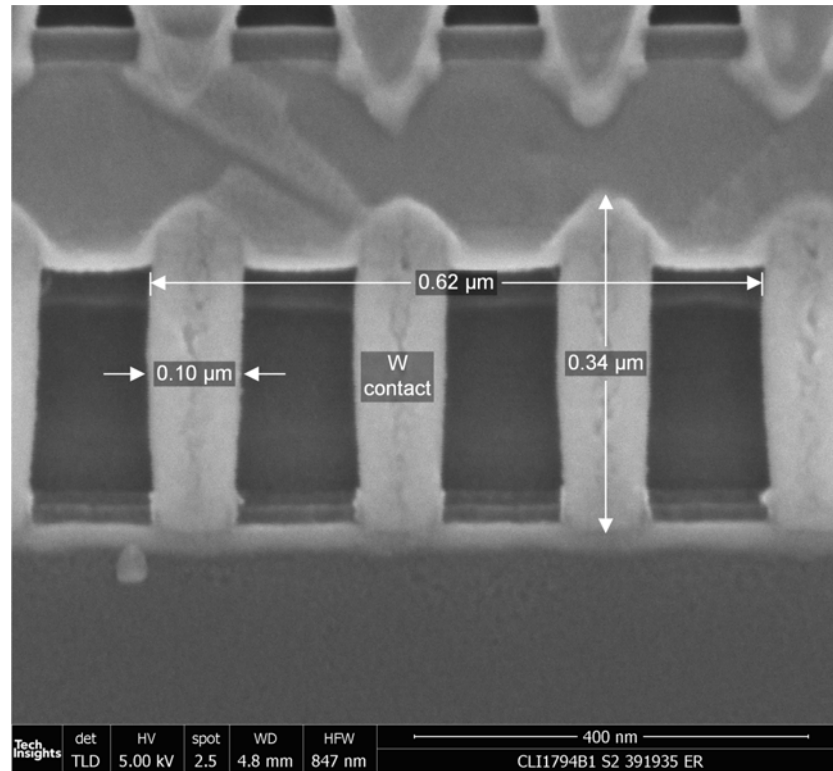
253_Block-6_Wells_15K_391935.png



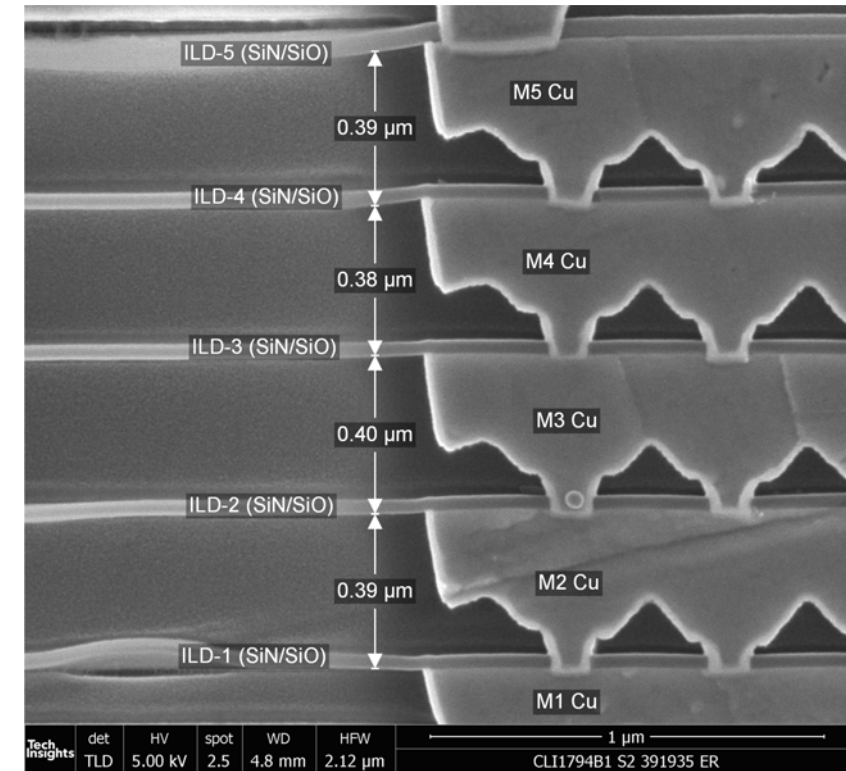
256_Block-6_Wells_40K_391935.png

Contacts & Interlevel Dielectric Layers – SEM Cross-Section

- Inter-metal vias (made of W) are $0.10\text{ }\mu\text{m}$ wide and $0.34\text{ }\mu\text{m}$ thick, with a pitch of $\sim 0.21\text{ }\mu\text{m}$.
- Interlayer dielectric layers have an average thickness of $\sim 0.39\text{ }\mu\text{m}$.



Contacts



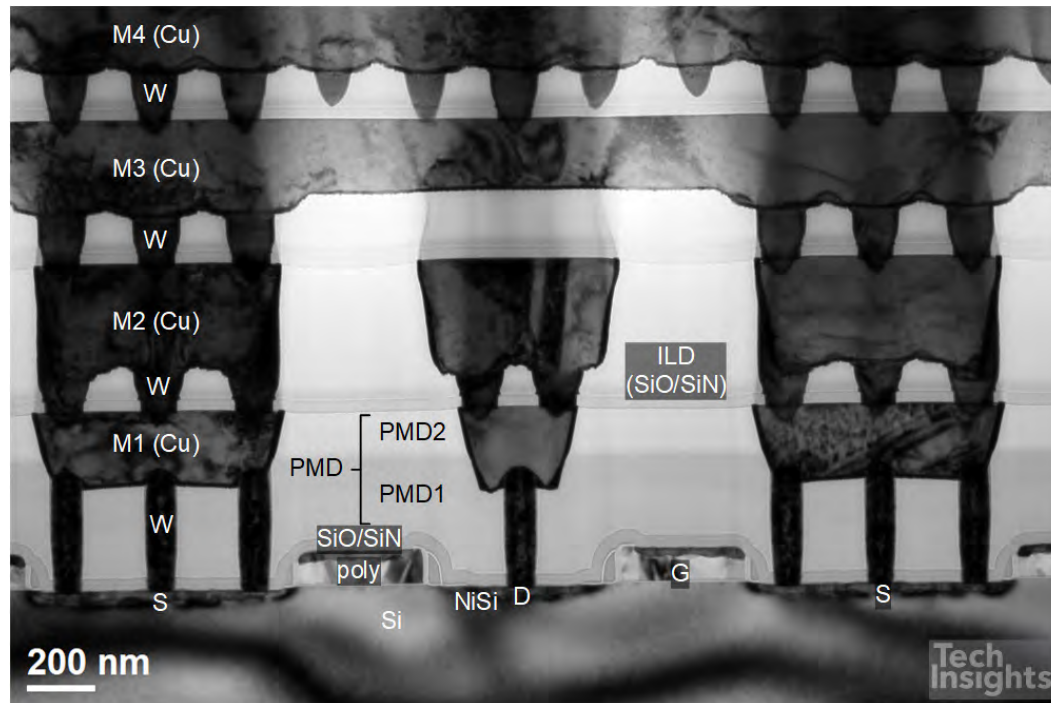
Interlevel Dielectric Layers

Die Cross-Sectional Analysis – Power Block

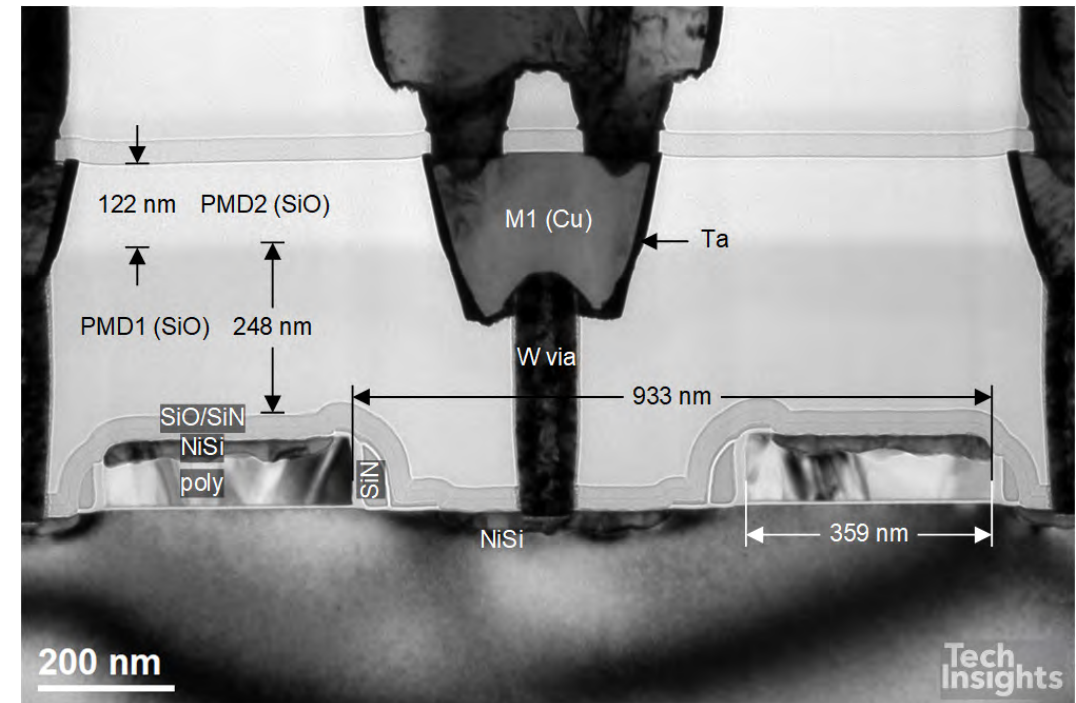
Part 2. TEM

Power Transistors (General View) – TEM Cross-Section

- General structure of the transistors consists of triple and single W vias (with tantalum (Ta) walls) for source and drain, respectively, polysilicon gates (Si) covered with an SiO/SiN contact etch stop layer (CESL), and a dual layer pre-metal dielectric (PMD; SiO) between the CESL and the first interlayer dielectric (ILD; SiO/SiN).



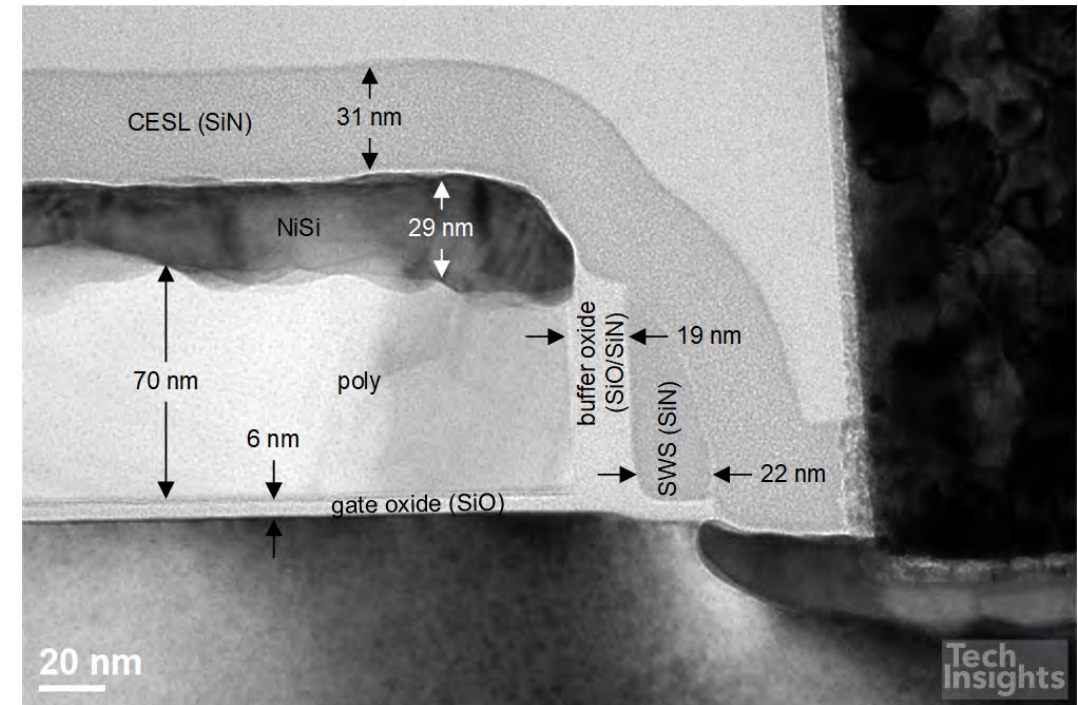
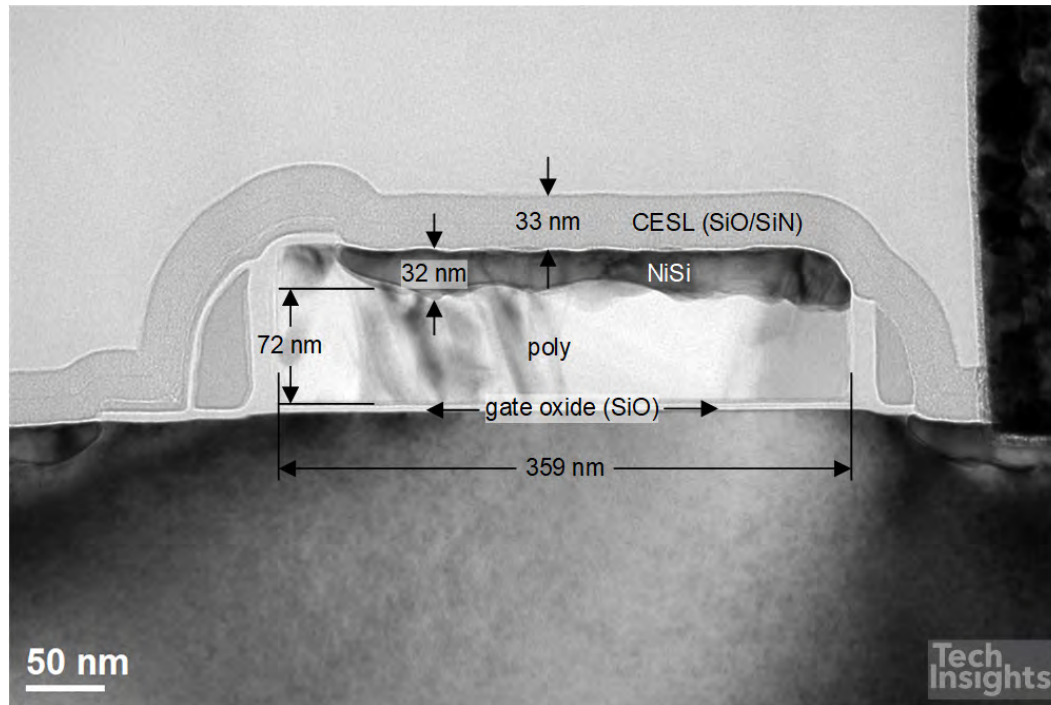
Transistor_8,9Kx_397339.png



Transistor_17,5Kx_397339.png

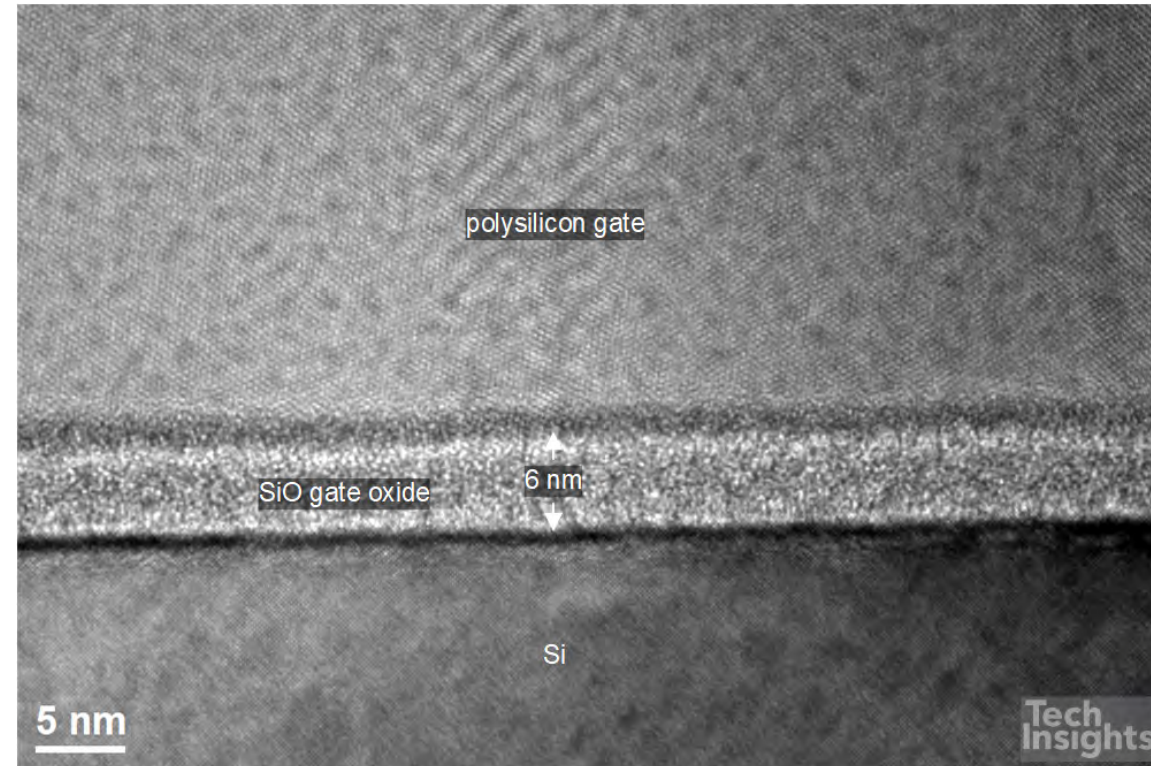
Power Transistors (Gate) – TEM Cross-Section

- The polysilicon gate is ~70 nm thick and 359 nm wide, covered with a 20-30 nm NiSi and ~31-33 nm CESL (made of SiN).
- Gate oxide is formed as a 6 nm layer made of SiO.



Power Transistors (Gate Oxide) – TEM Cross-Section

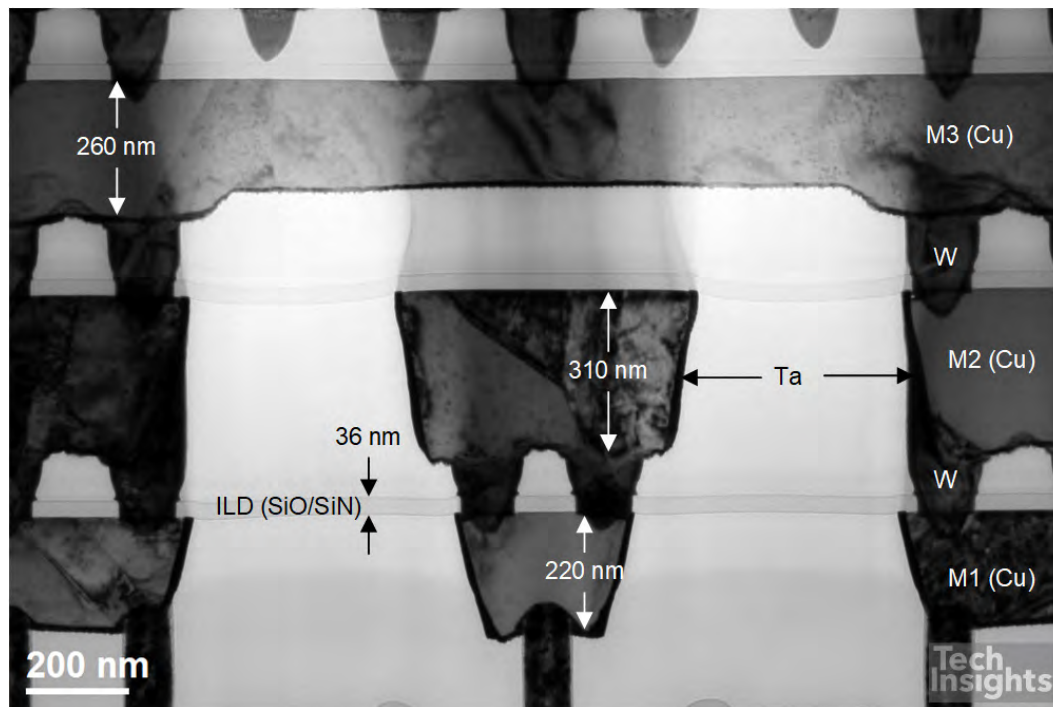
- Gate oxide is made of SiO with a 6 nm thickness.



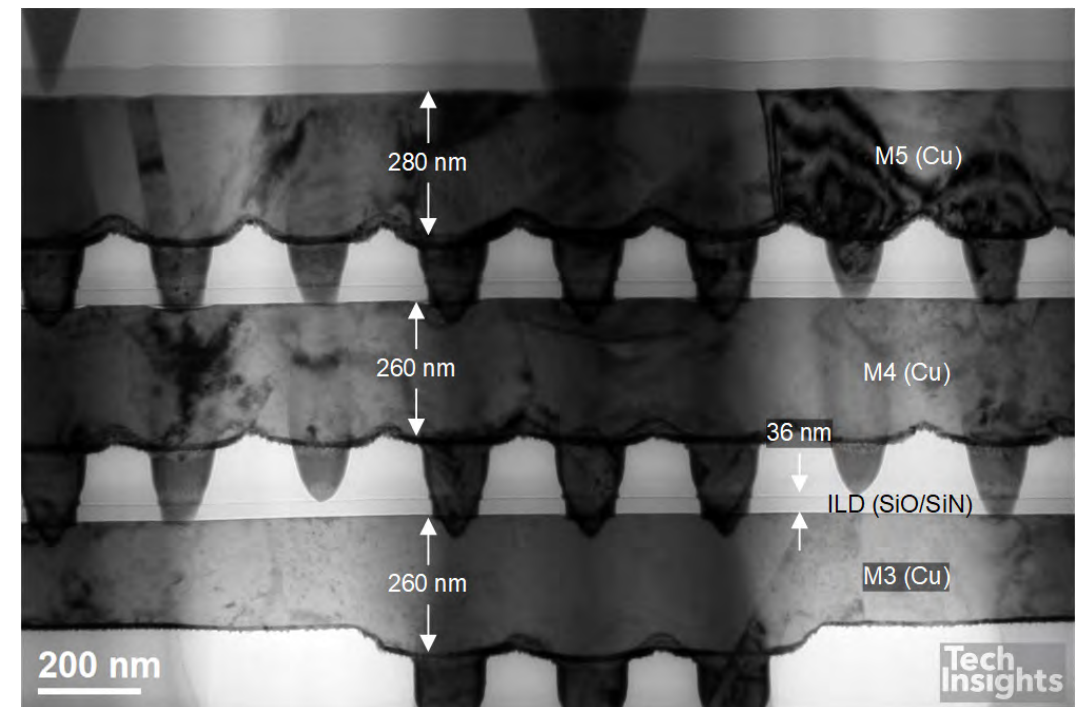
Transistor_Gox_410Kx_397339.png

Power Transistors (Metal Interconnect) – TEM Cross-Section

- Metal interconnects (Cu body with Ta walls) have various thicknesses, where at their thickest part one can estimate 220 nm for M1, 310 nm for M2, 260 nm for M3 and M4, and 280 nm for M5.
- Interlevel dielectric (ILD) layers are made of SiO/SiN and have an identical thickness of 36 nm.
- Metal interlayer contacts are made of W body with Ta walls.



M1-M3_13,5Kx_397339.png

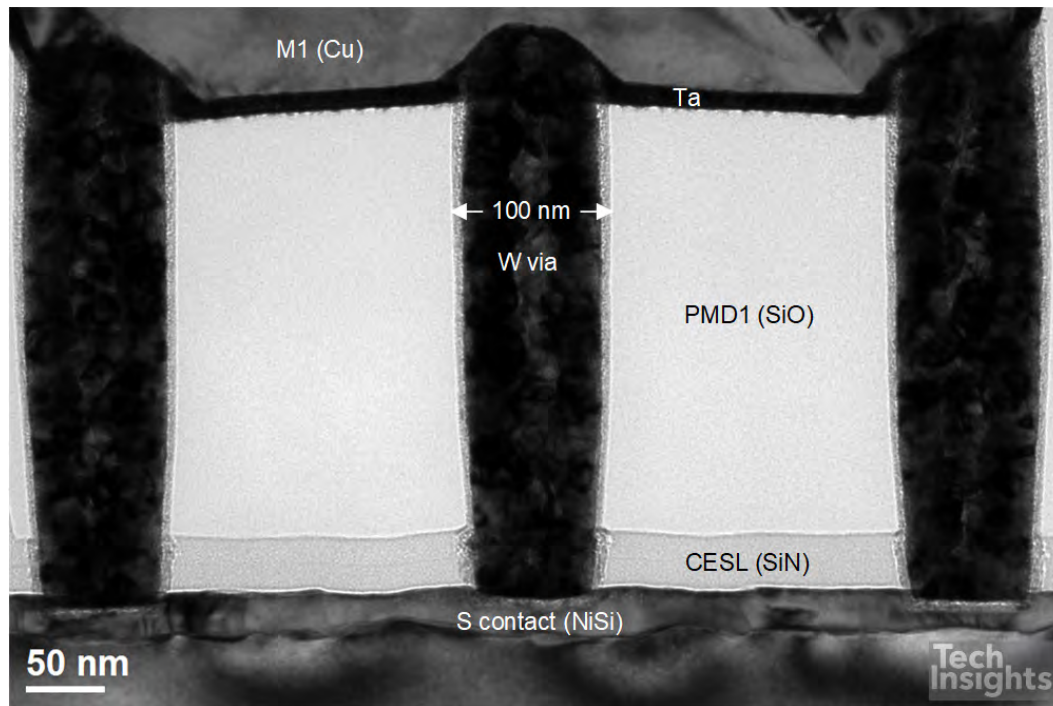
M1 – M3

M3-M5_13,5Kx_397339.png

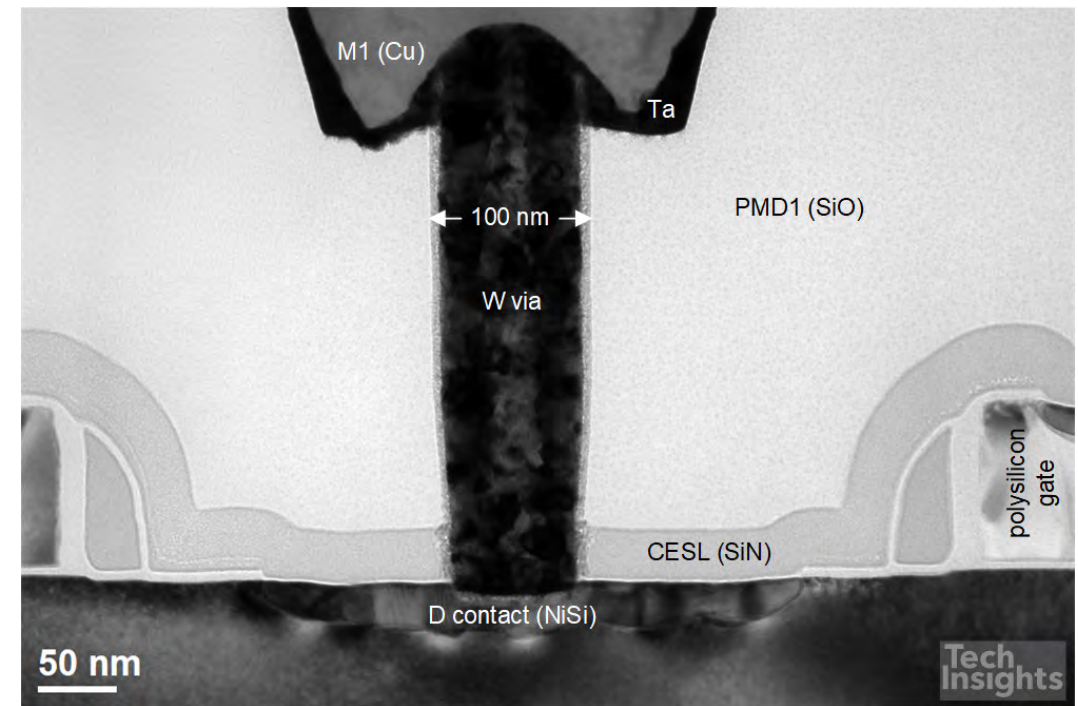
M3 – M5

Contacts & Vias – TEM Cross-Section

- Source and drain contacts are similarly made of NiSi.
- Source has three W vias and drain has one W via, all approximately 100 nm wide.



Contact_2_39Kx_397339.png

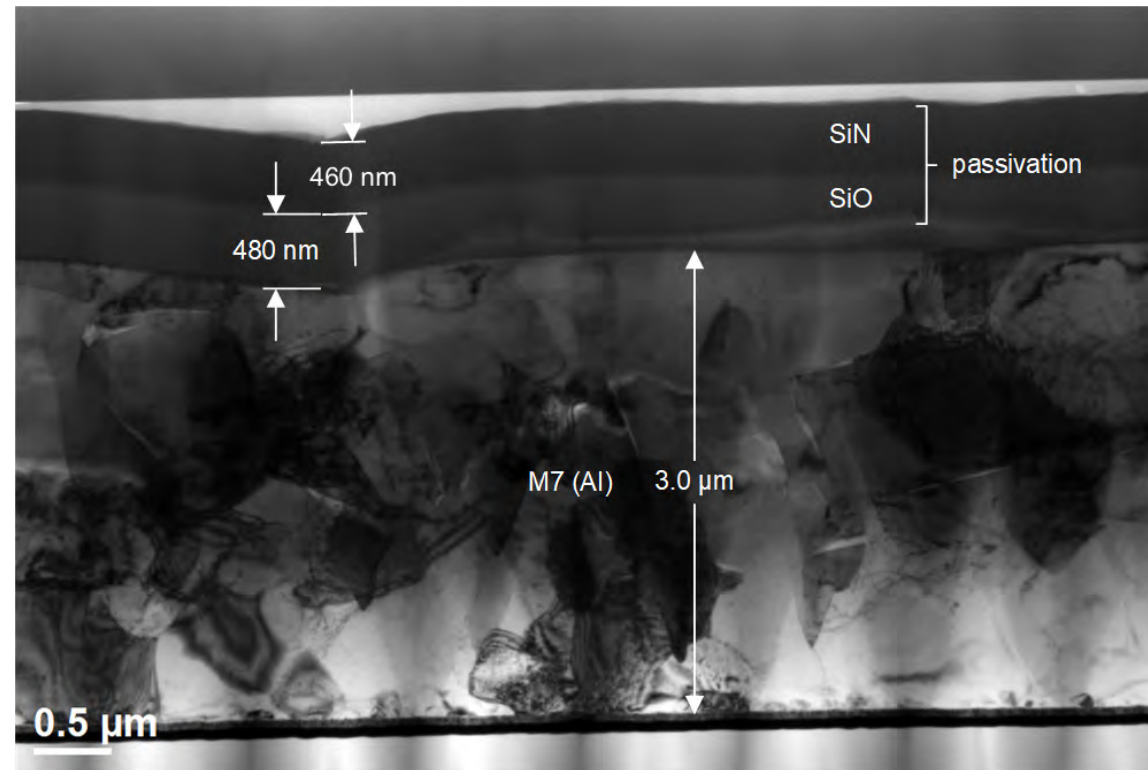
Source Contact

Contact_1_39Kx_397339.png

Drain Contact

Passivation – TEM Cross-Section

- The die features two-layer passivation in this region, measuring ~940 nm on top of M7 (Al, 3.0 μm).
- The passivation consists of two layers, with the inner layer made of SiO (480 nm) and the outer layer is made of SiN (460 nm).



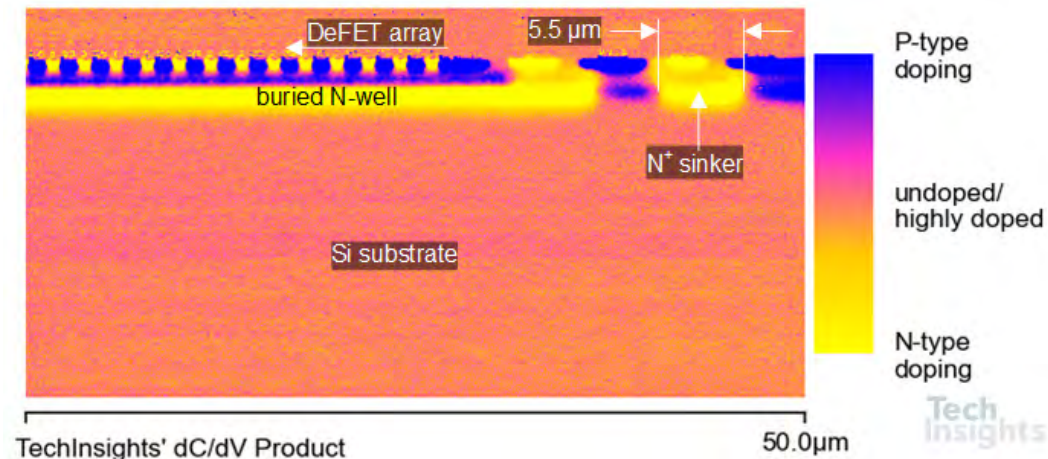
M7_3,6Kx_397339.png

Die Cross-Sectional Analysis – Power Block

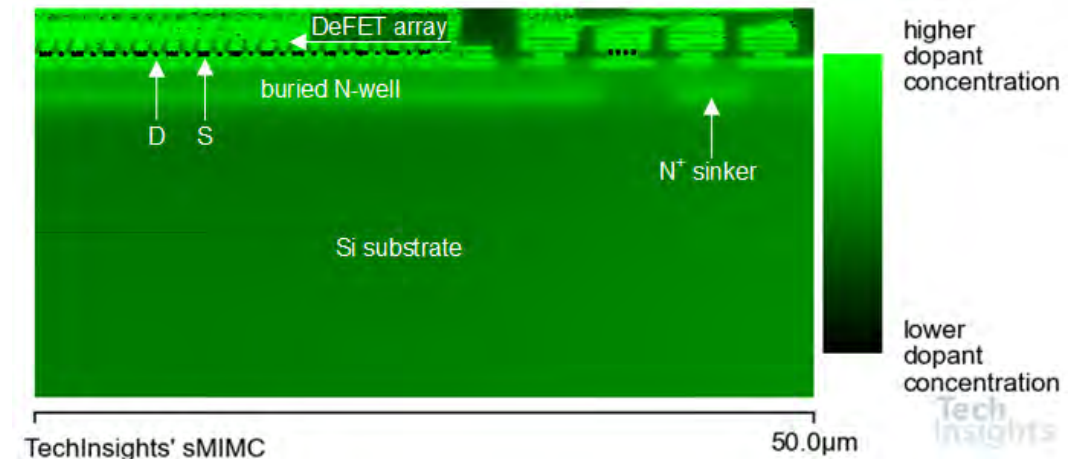
Part 3. SPM/sMIM

Power Block SPM/sMIM Analysis – Cross-Section

- The SPM/sMIM data shows a buried N-well layer (likely not epitaxially grown layers due to its non-uniformity on the Si substrate) formed on the Si substrate top. sMIM image on the right suggests that this layer is comprised of two sublayers, with the one closer to the Si substrate with a higher level of doping.
- The DeMOSFET layer is also made of sequences of S and D, with S characterized from its triple contacts (NiSi) on the sMIM image, whereas that of the drain is singular.
- Note that SCM imaging (such as the left image) is sensitive to the dopant type, with N-type material giving a negative (yellow) response, and P-type material giving a positive (purple) response.
- sMIM imaging (such as the right image) is sensitive to the dopant concentration level, with greater signal (brighter) corresponding to a higher dopant level, regardless of conductivity type.



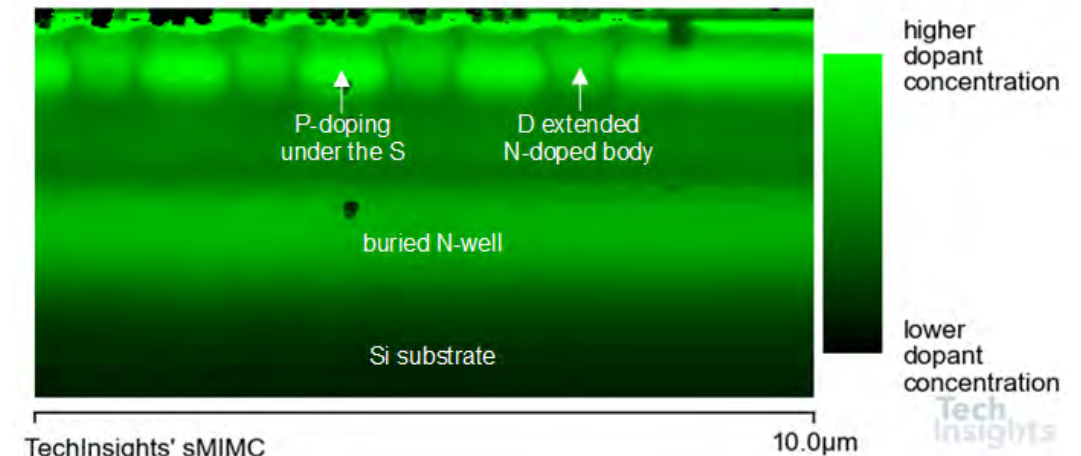
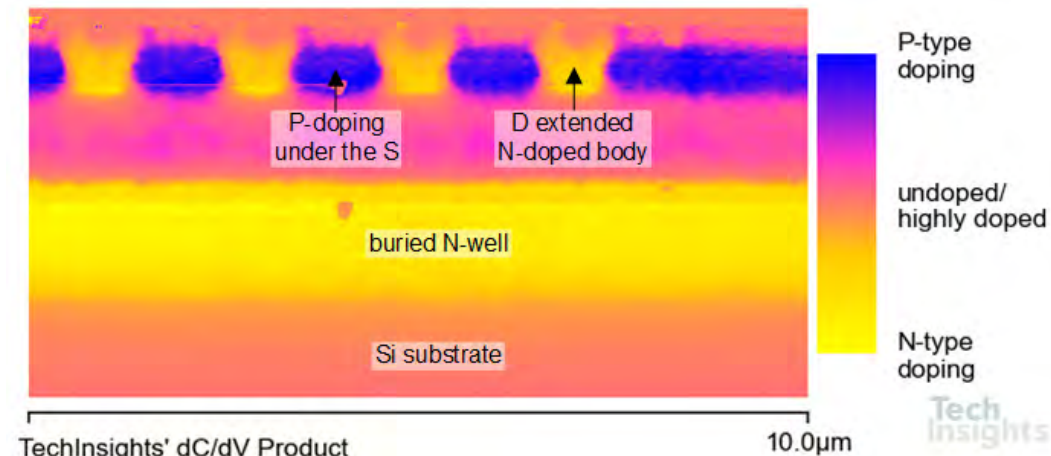
Block4_020722110040_PRODUCT_FRW_50.0u_512p_391935.png



Block4_020722110040_SMIMC_FRW_50.0u_512p_391935.png

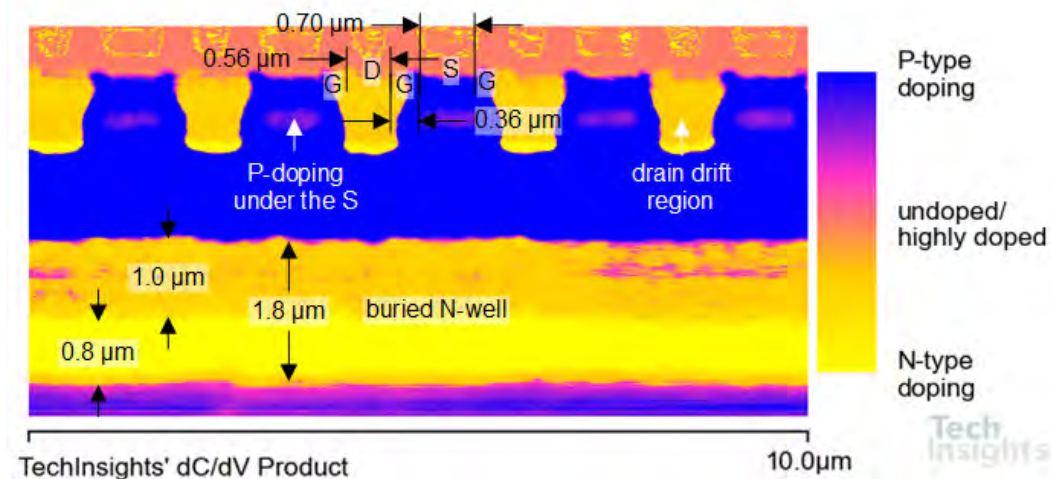
Power Block SPM/sMIM Analysis – Cross-Section

- The higher magnification SPM/sMIM images show a large N-doped block under the drain that is located farther from the gate, supportive of the DeMOSFET structure.
- Under the source, there are blocks of highly P-doped wells, which appear to be on top of a lightly P-doped layer. This P-doped layer is of course located on top of the buried N-well.

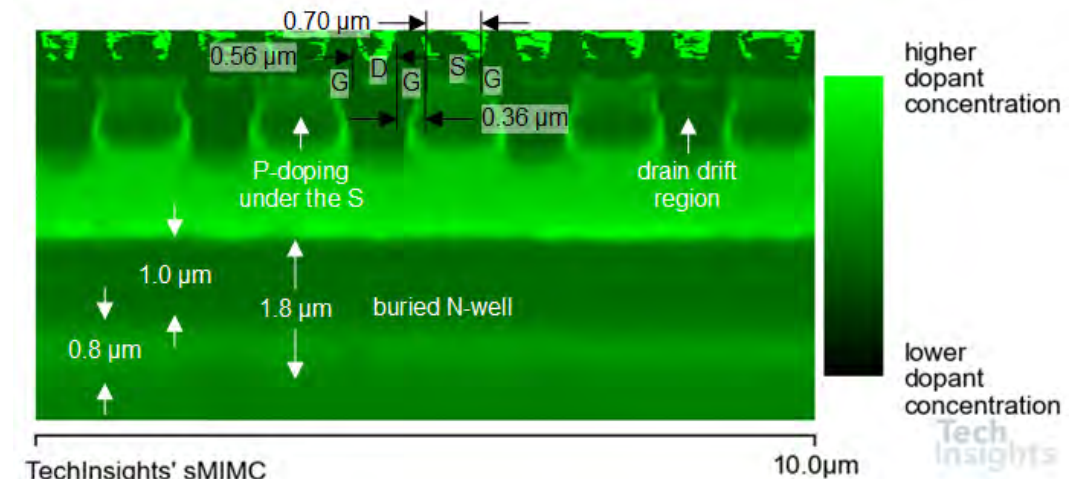


Power Block SPM/sMIM Analysis – Cross-Section

- The buried N-well appears to consist of two sublayers:
 - The top layer with lighter N-doping is 1.0 μm thick.
 - The bottom layer has a higher N-doping with 0.8 μm thickness.
- For each source, one can see two gates with P-doping underneath surrounding the source. The source appears to have a narrow N-doped layer, while drain is embarked on top of a large N-doped well.



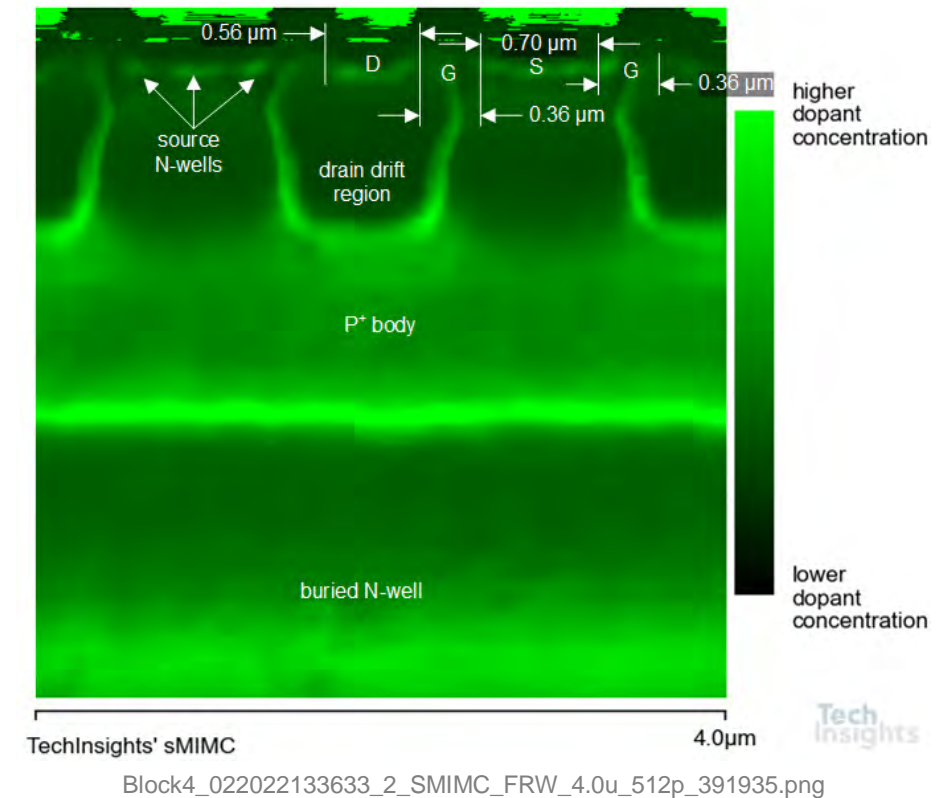
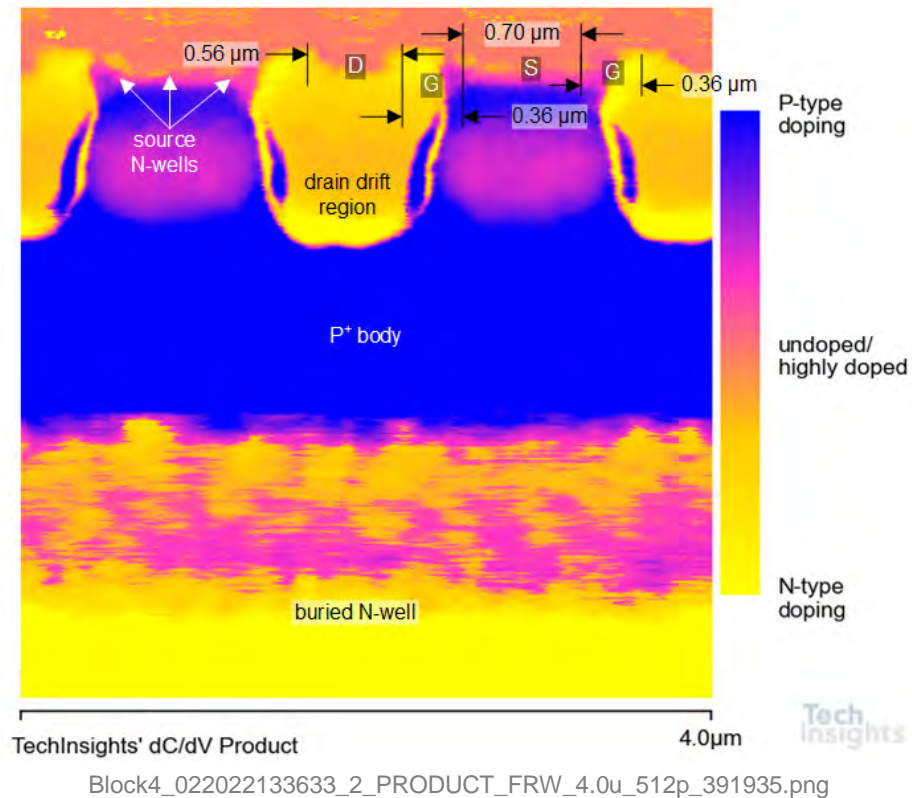
Block4_022022110933_1_PRODUCT_FRW_10.0u_512p_391935.png



Block4_022022110933_1_SMIMC_FRW_10.0u_512p_391935.png

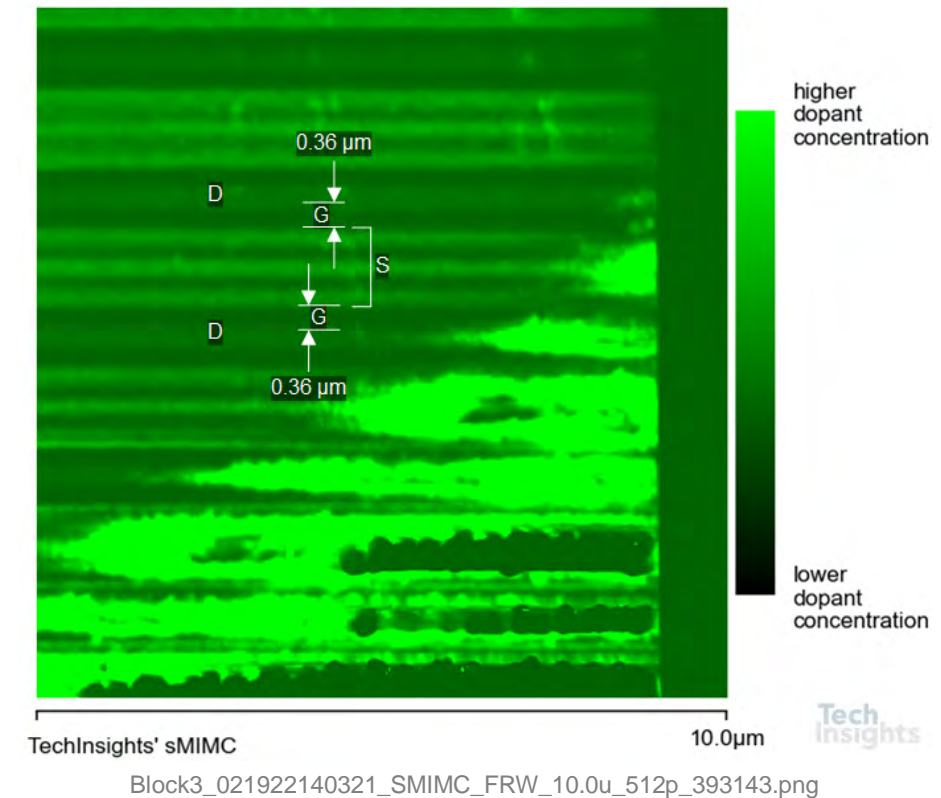
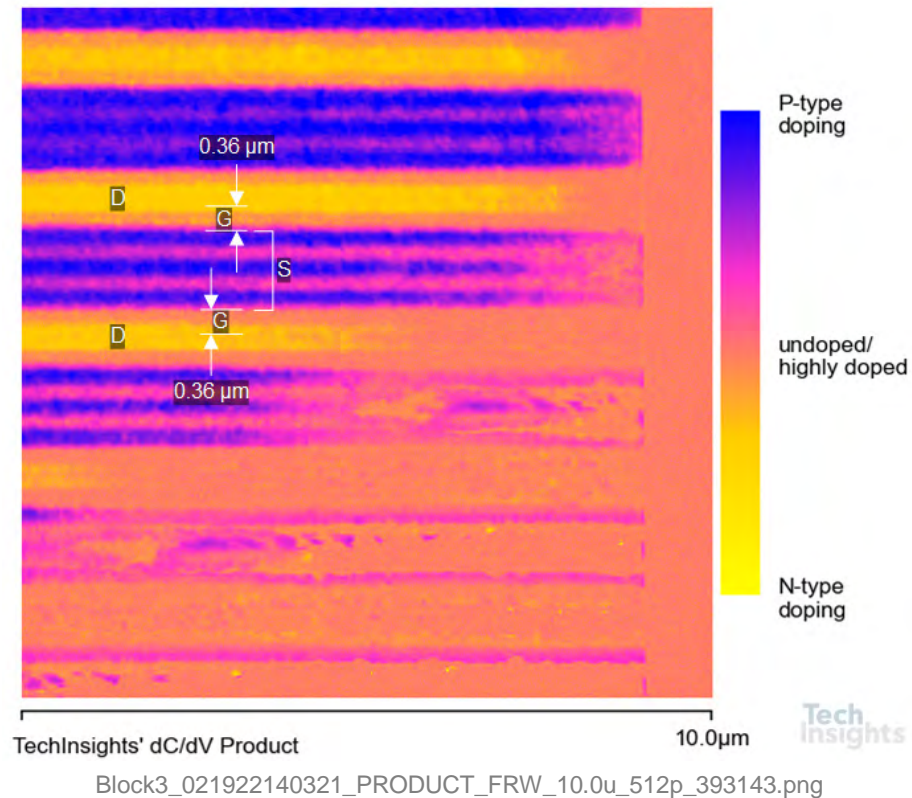
Power Block SPM/sMIM Analysis – Cross-Section

- Here one can (more) safely claim to see three source N-wells within the large P-well under the source. These are more obvious in the sMIM. The gates are on small P-doped wells, located closer to the source. These observations appear consistent with a DeMOSFET structure.



Power Block SPM/sMIM Analysis – Bevel

- Bevel view of the transistors show the location of source and drain. Gates can be seen as narrow bands attached to the outer source contacts.



Comparison with Maxim MAX77838 PMIC 90 nm BCD

- The Cirrus Logic CLI1793B1 analyzed in this report has functional similarity (PMIC) to the Maxim MAX77838 [4], therefore, a comparison of the two PMIC dies would be of interest. This comparison is limited to the structural properties of the two dies, since no application specific information is available for the Cirrus Logic CLI1793B1 die.

| Feature | Cirrus Logic CLI1793B1 PMIC 55 nm BCD | Maxim MAX77838 PMIC 90 nm BCD |
|---------------------------------|---------------------------------------|-------------------------------|
| Device type | PMIC | PMIC |
| Transistors' type/configuration | DeMOSFET | VDMOS and DeMOS |
| Active substrate material | Si | P-type Si |
| Minimum contacted gate pitch | 0.26 μm | 0.43 μm |
| Minimum metal pitch | 0.18 μm | 0.25 μm |
| Process generation & type | 55 nm BCD | 90 nm BCD |
| Die foundry | GlobalFoundries | Maxim |
| Silicide | Ni-based | Co-based |
| Pre-metal dielectric (PMD) | SiO | SiO-SiOP |
| Die marking date | 2021 | 2014 |
| Wafer size | (Likely) 300 mm | 200 mm |
| Die size (whole die) | 3.70 mm x 5.07 mm | 2.56 mm x 2.21 mm |
| Overall substrate thickness | 279-290 μm | 270 μm |

References

- [1] “Apple Inc.”, New World Encyclopedia, https://www.newworldencyclopedia.org/entry/Apple_Inc. (accessed February 26, 2022)
- [2] “Company Overview”, Cirrus Logic website, <https://investor.cirrus.com/company-overview/default.aspx> (accessed February 24, 2022)
- [3] “Deep Dive Teardown of the Apple iPhone 13 Pro Max A2484 Smartphone”, *TechInsights*, [DDT-2109-824](#), December 31, 2021 (original published date)
- [4] “Maxim MAX77838 PMIC 90 nm BCD Process Review”, *TechInsights*, [PRR-1607-801](#), September 2, 2016 (original published date)

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm ($\pm 1.4\%$) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within $\pm 2\%$ of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a stage micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 μ m (0.3%) for the stage micrometer's 100 μ m pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately $\pm 5\%$ or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis is usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

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Revision History

| Revision | Published Date | Page | Description |
|----------|----------------|-------|---|
| 1.0 | March 8, 2023 | 6, 47 | Table, row “Die foundry”, changed “TSMC” to “GlobalFoundries” |